

Curriculum Vitae: Prof. Mark B. Josephs SMIEEE FBCS CITP

Membership of Professional and Learned Societies.....
Employment History.....
Visiting Positions.....
University Education.....
Research Grants.....
Industrial Consultancy.....
Teaching Experience.....
Predoctoral and Postdoctoral Supervision.....
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Membership of Professional and Learned Societies

Chartered Fellow (elected November 2004) of the British Computer Society (BCS);
Member (elected February 2004) of the UK Computing Research Committee (UKCRC), an expert panel of the BCS, the Institution of Engineering and Technology (IET), and the Council of Professors and Heads of Computing (CPHC); serving on its Membership Panel (elected February 2007);
Senior Member (elected March 2001) of the Institute of Electrical and Electronics Engineers (IEEE), subscribing to its Computer Society and its Communications Society.

Employment History

London South Bank University

Professor of Computing (since 1998), with the following management rôles:

- ◆ Director (since 2005), Institute for Computing Research — the Institute consolidates all computing-related research centres within the Faculty;
- ◆ Member (since 2005), University Research Committee, RAE Working Group and SRIF Working Group; Member (since 2001), University Appointments Panel; Member (since 1999), University Research Degrees Committee and its Engineering, Science & Technology Sub-Committee;
- ◆ Head (2001-2003), Division of Computer Architecture & Data Processing;
- ◆ Director of Academic Disciplines (1997-2001), School of Computing;

Reader (1994-1998);

Principal Lecturer (1993), establishing the Centre for Concurrent Systems & VLSI.

University of Oxford

Member (1988-1995), Faculty of Mathematical Sciences;

Research Officer (1988-1993), Computing Laboratory;

Lecturer in Computation (1988-1993), Trinity College;

Research Officer (1986), Computing Laboratory.

Visiting Positions

Visiting Associate (Autumn 2005), Computer Science Department, California Institute of Technology;
Visiting Fellow (Summer 1990), Department of Mathematics and Computing Science, Eindhoven University of Technology;
Visiting Scientist (throughout 1987) and Academic Visitor (Summer 1988), IBM Research Division, Yorktown Heights.

University Education

DPhil in Computation, Wolfson College, Oxford, June 1986;
MSc in Computation, Wolfson College, Oxford, September 1984;
BSc (Hons) in Mathematics, University College, London, June 1983.

Research Grants

Conference Grant, 2006/R4 — awarded £1,100 by the Royal Society, 2007;
Overseas Travel Grant for Development of Collaborations with Caltech and NASA/JPL, EP/D050529 — awarded £10,601 by UK EPSRC, 2005-2006, and rated "tending to internationally leading" (for research quality and for research planning and practice) and "tending to outstanding" (overall);
Overseas Travel Grant for EuroSoC FP6 NoE Proposal Preparation, GR/S47151 — awarded £1,600 by UK EPSRC, 2003, and rated "tending to internationally leading" (for research planning and practice) and "tending to outstanding" (overall);
Working Group on Asynchronous Circuit Design (ACiD-WG), EP:IST-1999-29119, FP5 — awarded €465,000 by European Commission, 2000-2005;
Translation from Delay-Insensitive Algebra into Petri Nets, with Application to Asynchronous Circuit Design, GR/M51567 — awarded £46,590 by UK EPSRC, 1999-2000, and rated "tending to internationally leading" (for research quality and for research planning and practice) and "tending to outstanding" (overall);
Working Group on Asynchronous Circuit Design (ACiD-WG), EP:21949, FP4 — awarded 275,000 ECU by European Commission, 1996-2000;
Self-Timed Asynchronous Packet Router Design, GR/H77736 — awarded £108,000 by UK SERC, 1993-1996, and rated alpha 3;
Working Group on Asynchronous Circuit Design (ACiD-WG), EP:7225, FP3 — awarded 250,000 ECU by European Commission, 1992-1995;
Exploitation of Asynchronous Circuit Technologies (OMI/EXACT), EP:6143, FP3 — awarded 260,000 ECU by European Commission, 1992-1995;
Academic Research Collaboration Travel Grant to visit the Technical University of Denmark — awarded £490 by the British Council, 1991.

Industrial Consultancy

IBM Hursley Park — advised and assisted in the use of formal methods (particularly Z) applied to transaction processing systems (such as CICS) and object-oriented information systems, 1990-1996;
JMA Information Engineering — advised on the integration of formal and structured methods, 1992-1993;
LBMS — investigated the relationship between Z and LBMS Systems Engineering, 1991;
IBM Winchester — compared Z with an in-house method for software development, 1989-1990.

Teaching Experience

London South Bank University

Commercial Networked Environments

— Level M, MSc Business Information Technology, 2007;

Internet Technologies — Level M, MSc Internet and Database Systems, 2006;

Operating Systems: Scheduling & Storage, and

Operating Systems: Input/Output & Networks

— Level 2, BSc Computing Studies, and BSc Internet Computing, 1999-2005;

Concurrent Systems — Level 3, BSc Computing Studies, 1996-1999;

Microprocessor Technology — Level 2, BSc Computing Studies, 1996-1997 and 1999;

Computing Mathematics — Level 2, BSc Computing Studies, 1995-1996.

University of Oxford

Asynchronous Systems and Circuits

— MSc Computation, BA Mathematics and Computation, and

BA Engineering and Computing Science, 1993-1995;

Elements of Computer Programming — MSc Computation, 1989-1991;

Tutorials in Functional Programming, Logic, Computer Systems Architecture,

Software Engineering, Distributed Computing, and Algorithm Design

— BA Mathematics and Computation, and BA Engineering and Computing Science,

at Trinity, Magdalen and Pembroke Colleges, 1988-1993.

Predocctoral and Postdoctoral Supervision

London South Bank University

Dennis Furey (since 1998) Postdoctoral Research;

Ali Haidar and Mark Campbell (both since 2006, as 2nd supervisor) Predocctoral Research;

Mohsen Naderi (2005-2006) Predocctoral Research;

Hemangee Kapoor (2001-2004) PhD in “Delay-Insensitive Processes: A Formal Approach to the Design of Asynchronous Circuits”;

Kalpesh Kapoor (2001-2004, as 2nd supervisor) PhD in “Stability of Test Criteria and Fault Hierarchies in Software Testing”;

Issam Damaj (2001-2004, as 2nd supervisor) PhD in “Synthesis of Parallel Algorithms for Field Programmable Gate Arrays, with Applications from Cryptography”;

Igor Lemberski (2000-2002) Postdoctoral Research;

Jun Xu (1998-2002) PhD in “Asynchronous Interconnection and Interfacing of Intellectual Property Cores in the Design of Systems-on-Chip”;

Francesco Pessolano (1997-2000) PhD in “Heterogeneous Clustered Processors: Organization and Design”;

Phillip Burrell (1996-1997) PhD by Publication in “The Hybrid Approach of Decision-Support Technology”;

Mark Jarvis (1994-1996) Predocctoral Research;

Andrew Storey (1994-1995) PhD in “From B to SPARK”;

Shannon Morton (1994-1995) Predocctoral Research;

Sylvia Jennings (1994-1995) Postdoctoral Research.

University of Oxford

C.G. Huang (1994-1995, second supervisor) Postdoctoral Research;
Mick Patrick (1993) Predoctoral Research;
Jun Ginbayashi (1992-1995) DPhil in “Formal Methods and Tools for Systems Analysis and Design”;
Janet Barnes (1990-1993) DPhil in “A Mathematical Theory of Synchronous Communication”;
MSc Dissertations: one, 1998/9; three, 1990/1; five, 1991/2; and six, 1992/3.

Research Presentations

2007 seminars, Universities of Surrey and California, Berkeley; IEEE symposium, Berkeley;
2006 BCS lecture (invited discussant); seminar, University of Oxford;
2005 seminars, Caltech and De Montfort University; workshops, Caltech and BCS specialist group; conference, St. Malo;
2004 IEEE symposium, Hersonissos (invited talk); ACM/IEEE conference, San Diego; BCS specialist group symposium (invited talk); workshop, Turku;
2003 seminar, LSBU; workshops, Manchester and Munich; IEEE symposium, Vancouver;
2002 summer school, Grenoble (lectures); workshop, Munich;
2001 workshops, Cambridge (tutorial) and Neuchatel;
2000 workshops, London (tutorial) and Grenoble;
1999 seminar, University of Reading; workshops, Newcastle and Lyon;
1998 seminars, University of Kent and South Bank University; workshops, Turin and St. Petersburg; conference, Marstrand;
1997 seminar, Imperial College; workshops, Newcastle, Edinburgh and London;
1996 seminar, University of Manchester; workshop, Groningen; IEEE symposium, Aizu;
1995 seminar, Racal; workshop, Sea of Galilee;
1994 seminars, Imperial College, Surrey University and Cambridge University; workshop, Aveiro; IEEE symposium, Utah;
1993 workshop, Barcelona (tutorial); IFIP working conference, Manchester; workshop, Lyngby; seminars, University of Oxford and South Bank University;
1992 seminars, MIT, IBM Yorktown Heights and Hewlett-Packard Laboratories, Bristol; workshops, Leuven and Lyngby;
1991 seminars, IBM Hursley Park, INMOS, SRI Cambridge, Technical University of Denmark, and the Universities of Groningen, Manchester, Surrey, Oxford, Cambridge and Edinburgh; workshop, Amsterdam;
1990 seminars, Philips Research Laboratories and Eindhoven University of Technology; IFIP working conference, Sea of Galilee; workshop, Rutgers University;
1989 seminars, Washington University, St. Louis, the University of Texas at Austin and IBM Yorktown Heights;
1988 seminars, Cambridge University and IBM Hursley Park;
1987 seminar, IBM Yorktown Heights.

International Academic Publications

Josephs MB, Kapoor HK (2007) Controllable Delay-Insensitive Processes. *Fundamenta Informaticae* 78(1):101-130, IOS Press. [Extended version of ACSD 2005 paper that was selected for special issue of journal.]
Josephs MB (2007) Gate-level modelling and verification of asynchronous circuits using

- CSP_M and FDR. In: *Asynchronous Circuits and Systems (Async)*, proceedings of the 13th IEEE Int'l Symp, pp 83-92, IEEE CS Press.
- Josephs MB, Jones C, Jackson M, et al. (2007) Discussion on The Ideal of Program Correctness by Tony Hoare, *The Computer Journal* 50(3):261-268, Oxford University Press.
- Xu J, Josephs MB, Sotudeh R (2006) Asynchronous Packet-Switching for Networks-on-Chip. In: *Application of Concurrency to System Design (ACSD)*, proceedings of the 6th Int'l Conf, pp 201-207, IEEE CS Press.
- Kapoor HK, Josephs MB, Furey DP (2006) Verification and Implementation of Delay-Insensitive Processes in Restrictive Environments. *Fundamenta Informaticae* 70(1-2):21-48, IOS Press. [Extended version of ACSD 2004 paper that was selected for special issue of journal.]
- Kapoor HK, Josephs MB (2005) Controllable Delay-Insensitive Processes and their Reflection, Interaction and Factorisation. In: *Application of Concurrency to System Design (ACSD)*, proceedings of the 5th Int'l Conf, pp 58-67, IEEE CS Press.
- Josephs MB (2005) Models for Data-Flow Sequential Processes. In: Abdallah AE, Jones CB, Sanders JW (eds) *Communicating Sequential Processes: The First 25 Years*, Festschrift, LNCS 3525, pp 85-97, Springer-Verlag.
- Kapoor HK, Josephs MB, Furey DP (2004) Verification and Implementation of Delay-Insensitive Processes in Restrictive Environments. In: *Application of Concurrency to System Design (ACSD)*, proceedings of the 4th Int'l Conf, pp 89-98, IEEE CS Press.
- Kapoor HK, Josephs MB (2004) Decomposing specifications with concurrent outputs to resolve state coding conflicts in asynchronous logic synthesis. In: *Design Automation (DAC)*, proceedings of the 41st Conf, pp 830-833, ACM.
- Kapoor HK, Josephs MB (2004) Modelling and verification of delay-insensitive circuits using CCS and the Concurrency Workbench. *Information Processing Letters* 89:293-296, Elsevier.
- Josephs MB (2003) An analysis of determinacy using a trace-theoretic model of asynchronous circuits. In: *Asynchronous Circuits and Systems (Async)*, proceedings of the 9th IEEE Int'l Symp, pp 121-130, IEEE CS Press.
- Josephs MB, Furey DP (2002) A programming approach to the design of asynchronous logic blocks. In: Cortadella J, Yakovlev A, Rozenberg G (eds) *Concurrency and Hardware Design: Advances in Petri Nets*, State-of-the-Art Survey, LNCS 2549, pp 34-60, Springer-Verlag.
- Lemberski I, Josephs MB (2002) Optimal Two-Level Delay-Insensitive Implementation of Logic Functions. In: Hochet B, Acosta AJ, Bellido MJ (eds) *Integrated Circuit Design*, LNCS 2451, pp 92-100, Springer-Verlag.
- Josephs MB (2001) Models of Asynchronous Computation. Chapter 16 in: Ashenden P, Mermet J, Seepold R (eds) *System on Chip Methodologies & Design Languages*, pp 187-192, Kluwer Academic Publishers. [FDL'99 paper that was selected for inclusion in book.]
- Josephs MB, Furey DP (2000) Delay-insensitive interface specification and synthesis. In: Marwedel P, Bolsens I (eds) *Design, Automation and Test in Europe (DATE)*, pp 169-173, IEEE CS Press.
- van Berkel CH, Josephs MB, Nowick SM (1999) Applications of Asynchronous Circuits. *Proceedings of the IEEE* 87(2):223-233, IEEE Press.
- Josephs MB, Nowick SM, van Berkel CH (1999) Modeling and Design of Asynchronous Circuits. *Proceedings of the IEEE* 87(2):234-242, IEEE Press.

- Nowick SM, Josephs MB, van Berkel CH (1999) Scanning the Special Issue on Asynchronous Circuits and Systems. *Proceedings of the IEEE* 87(2):219-222, IEEE Press.
- Josephs MB (1998) Formal derivation of a loadable asynchronous counter. In: Jeuring J (ed) *Mathematics of Program Construction (MPC)*, LNCS 1422, pp 234-253, Springer-Verlag.
- Josephs MB (1998) Book Review of "Protocol Specification, Testing & Verification XV". *Software Testing, Verification & Reliability* 8(1):49, Wiley.
- Josephs MB, Bailey AM (1997) The use of SI-Algebra in the design of sequencer circuits. *Formal Aspects of Computing* 9:395-408, Springer-Verlag.
- Josephs MB, Yantchev JT (1996) CMOS Design of the Tree Arbiter Element. *IEEE Trans. on Very Large Scale Integration (VLSI) Systems* 4(4):472-476, IEEE Press.
- Bush ME, Josephs MB (1996) Some Limitations to Speed-Independence in Asynchronous Circuits. In: *Advanced Research in Asynchronous Circuits and Systems (Async)*, proceedings of the 2nd Int'l Symp, pp 104-111, IEEE CS Press.
- Houston ISC, Josephs MB (1995) A formal description of the OMG's Core Object Model and the meaning of compatible extension. *Computer Standards & Interfaces* 17(5-6):553-558, North-Holland.
- Yantchev JT, Huang CG, Josephs MB, Nedelchev IM (1995) Low-Latency Asynchronous FIFO Buffers. In: *Asynchronous Design Methodologies*, proceedings of the 2nd Working Conf, pp 24-31, IEEE CS Press.
- Bailey AM, Josephs MB (1995) Sequencer Circuits for VLSI Programming. In: *Asynchronous Design Methodologies*, proceedings of the 2nd Working Conf, pp 82-90, IEEE CS Press.
- Houston ISC, Josephs MB (1994) Specifying distributed CICS in Z: accessing local and remote resources. *Formal Aspects of Computing* 6(5):569-579, Springer-Verlag.
- Josephs MB, Lucassen PG, Udding JT, Verhoeff T (1994) Formal Design of an Asynchronous DSP Counterflow Pipeline: A Case Study in Handshake Algebra. In: *Advanced Research in Asynchronous Circuits and Systems (Async)*, proceedings of the 1st Int'l Symp, pp 206-215, IEEE CS Press.
- Josephs MB, Udding JT (1993) An Overview of D-I Algebra. In: Mudge TN, Milutinovic V, Hunter L (eds) *System Sciences (HICSS)*, proceedings of the 26th Annual Hawaii Int'l Conf, pp 329-338, IEEE CS Press.
- Groenboom R, Josephs MB, Lucassen PG, Udding JT (1993) Normal Form in a Delay-Insensitive Algebra. In: Furber S, Edwards M (eds) IFIP Transactions A-28, *Asynchronous Design Methodologies*, pp 57-70, North-Holland.
- Josephs MB, Udding JT (1993) Implementing a stack as a delay-insensitive circuit. In: Furber S, Edwards M (eds) IFIP Transactions A-28, *Asynchronous Design Methodologies*, pp 123-135, North-Holland.
- Josephs MB, Mak RH, Udding JT, Verhoeff T, Yantchev JT (1992) High-Level Design of an Asynchronous Packet-Routing Chip. In: Staunstrup J., Sharp R. (eds) IFIP Transactions A-5, *Designing Correct Circuits*, pp 261-274, North-Holland.
- Josephs MB (1992) Receptive Process Theory. *Acta Informatica* 1:17-31, Springer-Verlag.
- Josephs MB, Udding JT (1991) An Algebra for Delay-Insensitive Circuits. In: Clarke EM, Kurshan RP (eds) DIMACS Series in Discrete Mathematics and Theoretical Computing Science 3, *Computer-Aided Verification '90*, pp 147-175, AMS-ACM.
- Josephs MB, Udding JT (1991) An Algebra for Delay-Insensitive Circuits (Abridged Version). In: Clarke EM, Kurshan RP (eds) *Computer-Aided Verification*, LNCS 531,

- pp 343-352, Springer-Verlag.
- Josephs MB, Udding JT (1990) Delay-Insensitive Circuits: An Algebraic Approach to their Design. In: Baeten JCM, Klop JW (eds) *CONCUR'90, Theories of Concurrency: Unification and Extension*, LNCS 458, pp 342-366, Springer-Verlag.
- Josephs MB, Udding JT (1990) The Design of a Delay-Insensitive Stack. In: Jones G, Sheeran M (eds) *Workshops in Computing, Designing Correct Circuits*, pp 132-152, Springer-Verlag.
- He Jifeng, Josephs MB, Hoare CAR (1990) A Theory of Synchrony and Asynchrony. In: Broy M., Jones C.B. (eds) *Programming Concepts and Methods*, pp 459-478, North-Holland.
- Josephs MB (1989) The Semantics of Lazy Functional Languages. *Theoretical Computer Science* 68:105-111, North-Holland.
- Josephs MB (1988) The Data Refinement Calculator for Z Specifications. *Information Processing Letters* 27:29-33, North-Holland.
- Josephs MB (1988) A State-Based Approach to Communicating Processes. *Distributed Computing* 3:9-18, Springer-Verlag.
- Josephs MB (1986) Functional Programming with Side-Effects. *Science of Computer Programming* 7:279-296, North-Holland.

Other Publications

Patent

- Houston ISC, Josephs MB (2001) Object-oriented data processing system with transactional adapter. US Patent 6,178,463, assigned to IBM.

Monograph

- Josephs MB (1986) *Functional Programming with Side-Effects*. Oxford University Programming Research Group Technical Monograph PRG-55, DPhil Thesis, 101 pages.

Contributions to Workshops

- Josephs MB (2005) Controllable Delay-Insensitive Processes. Abstract and slides in the proceedings of a *BCS-FACS Workshop* on Formal Methods and Testing, London.
- Naderi M, Josephs MB (2005) Using SPIN to Add Value to Asynchronous Hardware Design Flows. Extended abstract in the proceedings of the 17th *UK Asynchronous Forum*, University of Southampton.
- Kapoor HK, Josephs MB (2004) Wrappers that Weaken DI Processes. Extended abstract in the proceedings of the 16th *UK Asynchronous Forum*, University of Manchester.
- Kapoor HK, Josephs MB (2004) Verification and Implementation of Delay-Insensitive Processes in Restrictive Environments. Extended abstract in the proceedings of the 15th *UK Asynchronous Forum*, University of Cambridge.
- Kapoor HK, Josephs MB (2004) Automatically decomposing specifications with concurrent outputs to resolve state coding conflicts in asynchronous logic synthesis. Extended abstract in the proceedings of the 15th *UK Asynchronous Forum*, University of Cambridge.
- Kapoor HK, Josephs MB (2004) Decomposing Specifications to Resolve State Coding Conflicts in Asynchronous Logic Synthesis. Abstract and slides in the proceedings of an *ACiD-WG Workshop*, Turku.

- Kapoor HK, Josephs MB (2003) Computer-aided verification of delay-insensitive protocols. Abstract and slides in the proceedings of an *ACiD-WG Workshop*, Heraklion.
- Kapoor HK, Josephs MB (2003) Applying the Concurrency Workbench to the Verification of DI Circuits. Extended abstract in the proceedings of the 14th *UK Asynchronous Forum*, University of Newcastle.
- Furey DP, Josephs MB (2002) Asynchronous Circuit Design via Automated Petri Net Generation. Regular paper in the proceedings of a *Forum on Specification & Design Languages (FDL)*, Marseille.
- Josephs MB (2002) Verification of Delay-Insensitive Sequential Processes. Slides in the Lecture Notes of an *ACiD-WG Summer School*, TIMA Laboratory, Grenoble.
- Josephs MB (2002) Verification of a Loadable Counter. Slides in the Lecture Notes of an *ACiD-WG Summer School*, TIMA Laboratory, Grenoble.
- Josephs MB, Furey DP (2002) Asynchronous design using the DISP programming language and the tools di2pn and petrify. Abstract and slides in the proceedings of an *ACiD-WG Workshop*, Infineon Technologies, Munich.
- Kapoor HK, Josephs MB (2002) Automated Transformation of Delay-Insensitive Sequential Processes. Extended abstract in the proceedings of the 13th *UK Asynchronous Forum*, University of Cambridge.
- Josephs MB (2001) Self-Timed On-Chip Packet-Routing. Abstract and slides in the proceedings of an *ACiD-WG Workshop*, CSEM, Neuchatel.
- Josephs MB (2000) A Programming Language for Delay-Insensitive Communication. Tutorial in the proceedings of the 8th *UK Asynchronous Forum*, South Bank University, London.
- Josephs MB, Furey DP (2000) Delay-insensitive interface specification. In: Yakovlev A, Nouta R (eds) *Asynchronous Interfaces: Tools, Techniques and Implementations (AINT)*, proceedings of an Int'l Workshop, pp 75-80, Technical University of Delft, ISBN 90-5236-037-4.
- Josephs MB, Furey DP (2000) di2pn as a front-end to petrify. Abstract and slides in the proceedings of an *ACiD-WG Workshop*, TIMA Laboratory, Grenoble.
- Josephs MB (1999) Multithreaded Simulation of Petri Nets and Asynchronous Circuits. Extended abstract in the proceedings of the 7th *UK Asynchronous Forum*, University of Newcastle.
- Josephs MB (1999) Models of Asynchronous Computation. In: Mermet J, Seepold R (eds) *Design Languages (FDL)*, proceedings of the 2nd Int'l Forum, pp 472-476, ENS-Lyon, ISBN 2-84010-033-9.
- Josephs MB, Furey DP (1999) Developments in DI-Algebra: I/O Bursts & Integration with Petrify. Abstract and slides in the proceedings of an *ACiD-WG Workshop*, University of Newcastle, Computing Science Technical Report 670.
- Pessolano F, Josephs MB (1998) A low-power, high-speed stack controller designed using asynchronous circuit techniques. In: Trullemans-Anckaert A-M, Sparsø J (eds), *Power and Timing Modeling, Optimization and Simulation (PATMOS)*, proceedings of the 8th Int'l Workshop, pp 387-396, Technical University of Denmark, ISBN 87-89112-49-0.
- Furey DP, Josephs MB (1998) Translating DI-Algebra to Petri Nets. Extended abstract in the proceedings of the 5th *UK Asynchronous Forum*, University of Cambridge.
- Josephs MB (1998) Applying Handshake Algebra to the formal specification of sequential and pipelined versions of an asynchronous DLX processor. Abstract and slides in the proceedings of an *ACiD-WG Workshop*, Politecnico di Torino.

- Josephs MB (1998) Self-timed FSM Synthesis. Abstract and slides in the proceedings of a Special Interest Group Workshop on Exploitation of STG-based Design Technology, St. Petersburg State Electrotechnical University, Russia.
- Josephs MB (1997) A few suggestions on how to implement self-timed finite-state machines. Extended abstract in the proceedings of the 3rd *UK Asynchronous Forum*, University of Edinburgh.
- Josephs MB (1997) Formal derivation of a loadable asynchronous counter. Extended abstract in the proceedings of the 2nd *UK Asynchronous Forum*, University of Newcastle.
- Bush ME, Josephs MB (1996) Behavioural Modelling of Asynchronous Circuits. In: *Design and Test of Asynchronous Systems*, IEE Colloquium Digest 40, pp 6/1-6/6, London.
- Josephs MB (1996) Using Handshake Algebra to help solve the loadable counter problem. Abstract and slides in the proceedings of an *ACiD-WG Workshop*, University of Groningen, Computing Science Notes 9602.
- Josephs MB (1996) Designing an interrupt handler out of standard parts. Abstract and slides in the proceedings of an *ACiD-WG Workshop*, University of Groningen, Computing Science Notes 9602.
- Josephs MB (1995) Mixing delay models: speed-independence, delay-insensitivity and handshaking. Abstract and slides in the proceedings of an *Israel Workshop on Asynchronous VLSI*, Kibutz Genossar.
- Josephs MB (1995) Comments on Alain Martin's Approach. Abstract and slides in the proceedings of an *Israel Workshop on Asynchronous VLSI*, Kibutz Genossar.
- Josephs MB (1994) Asynchronous Implementations of Logic Functions and State-Machines. Abstract and slides in the proceedings of an *ACiD-WG Workshop on Testing and Design for Testability*, INESC-Aveiro.
- Josephs MB (1994) Event Register Specification and Decomposition. Slides in the proceedings of the *AMULETI Modelling Workshop*, Windermere.
- Josephs MB (1994) Lock FIFO Specification and Decomposition. Slides in the proceedings of the *AMULETI Modelling Workshop*, Windermere.
- Huang C, Josephs MB, Nedelchev IM, Yantchev JT (1994) Low-latency asynchronous FIFO buffers. Abstract and slides in the proceedings of an *ACiD-WG Workshop on Asynchronous Low-Power VLSI*, Technical University of Denmark, Technical Report ID-TR:1994-140, Lyngby.
- Josephs MB, Yantchev JT (1994) CMOS Design of Arbiter Circuits. Abstract and slides in the proceedings of an *ACiD-WG Workshop on Asynchronous Low-Power VLSI*, Technical University of Denmark Technical Report ID-TR:1994-140, Lyngby.
- Josephs MB, Udding JT (1993) An algebraic approach to asynchronous circuit design. Abstract and slides in the proceedings of an *ACiD-WG Workshop on Digital Signal Processing*, Universitat Politecnica de Catalunya, DAC Technical Report RR 93/24, Barcelona.
- Josephs MB (1992) Speed-independent design of a toggle. Abstract and slides in the proceedings of an *ACiD-WG/EXACT Workshop on Asynchronous Controllers and Interfacing*, IMEC Technical Report EXACT/D.2/IMEC/m3/D1, Leuven.
- Josephs MB, Mak RH, Verhoeff T (1991) Asynchronous Design of a Router. In: Veen JP (ed) *Circuits, Systems and Signal Processing*, proceedings of the IEEE/ProRISC Symp, pp 173-179, STW Utrecht, ISBN 90-73461-02-2, Veldhoven.
- Redmond-Pyle D, Josephs MB (1991) Enriching a Structured Method with Z. Regular paper in the proceedings of the *Methods Integration Conference*, Leeds.

I have also (co-)authored Technical Reports at Eindhoven University of Technology, the University of Groningen, the University of Oxford, London South Bank University, Washington University, St. Louis, and IBM Yorktown Heights.

Other Professional Activities

Workshop/Conference Committee Membership/Chairs

National-level

Member (1997-2005), Steering Committee, UK Asynchronous Forum;
Organizer, 8th UK Asynchronous Forum, London, June 2000, and 12th UK Asynchronous Forum, London, June 2002.

European-level

Chair (1992-2005), Working Group on Asynchronous Circuit Design (ACiD-WG), supported by the European Commission;
Co-organizer of 13 ACiD-WG Workshops: Leuven, September 1992; Veldhoven, December 1992; Barcelona, September 1993; Lyngby, April 1994; Aveiro, November 1994; Groningen, September 1996; Turin, January 1998; Newcastle upon Tyne, January 1999; Grenoble, January 2000; Neuchatel, February 2001; Munich, January 2002; Heraklion, January 2003; Turku, June 2004;
Co-organizer of three ACiD-WG Schools: Lyngby, August 1997; Grenoble, July 2002; Cambridge, January 2005.

International-level

Member (1996-2007), Steering Committee, IEEE Int'l Symp. on Asynchronous Circuits & Systems (Async);
Co-Chair, 5th Async, Barcelona, April 1999;
Co-Chair, Programme Committee, 3rd Async, Veldhoven, April 1997;
Member, Programme Committee, of eleven Async Symposia: Aizu, March 1996; Veldhoven, April 1997; San Diego, March 1998; Barcelona, April 1999; Eilat, April 2000; Vancouver, May 2003; Hersonissos, April 2004; New York, March 2005; Grenoble, March 2006; Berkeley, March 2007; Newcastle upon Tyne, April 2008;
Chair, 2nd Working Conference on Asynchronous Design Methodologies, London, May 1995, supported by ACiD-WG and the IEEE Computer Society Technical Committee on VLSI;
Member, Programme Committee, 1st Working Conference on Asynchronous Design Methodologies, Manchester, March 1993, supported by IFIP Working Group 10.5 and ICL;
Member, Programme Committee, Special Session on Formal Methods for Engineering Special-Purpose Parallel Systems, IEEE Int'l Conf. on Electronics Circuits and Systems, Kaslik, Lebanon, December 2000;
Member, Programme Committee, of five Int'l Conferences on Application of Concurrency to System Design (ACSD): Newcastle-upon-Tyne, June 2001; Guimarcos, Portugal, June 2003; St. Malo, June 2005; Turku, June 2006; Bratislava, Slovakia, July 2007.

Editorial Role

Guest co-editor, Special Issue on Asynchronous Circuits and Systems, Proceedings of the IEEE, February 1999.

External Examiner

Lucassen P, PhD, University of Groningen, 1994;
Farnsworth C, MSc, University of Manchester, 1994;
Molina P, PhD, Imperial College, London, 1997;
Hooker S, PhD, University of Teeside, 1997;
Bardsley A, MPhil, University of Manchester, 1998;
Meehan A, PhD, University of Ulster, 1999.

Reviewer

Reviewer of book proposals for several publishers, as well as submissions to various IEEE, IEE and Springer-Verlag journals and to numerous workshops/conferences;
Reviewer of research grant/fellowship proposals for national funding bodies and learned societies (in the UK, the Netherlands and Ireland).