

# INFORMATION SOCIETY TECHNOLOGIES (IST) PROGRAMME



Contract for:

**Concerted Action/Thematic Network**

## *Periodic Report 2*

Project acronym: ACiD-WG

Project full title: Working Group on Asynchronous Circuit Design

Contract no.: IST-1999-29119

Period: 1 September 2001 - 31 August 2002

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## 1. Project summary

### **Objectives**

ACiD-WG aims at improving the systematic exchange of information and the forging of links between teams which carry out RTD or take-up activities around the theme of asynchronous circuit design. Its objectives in FP5 are as follows:

1. **To encourage excellence in science and technology research pertaining to asynchronous circuits and systems.**
2. **To facilitate the development of methods and tools that are usable by engineers for the design of asynchronous VLSI systems.**
3. **To promote the adoption of asynchronous circuit design in industry.**

### **Description of the work**

Four workshops will be organised, hosted by members of the Working Group and will take place in different member and associated states of the European Union, on the theme of asynchronous circuits and systems. Attendance and presentations by all members of the Working Group and by industrial affiliates will be encouraged. Invitations to participate will also be extended to non-members of the Working Group. In addition, visits between members will take place and special interest group meetings will be organised.

A summer school will be organised for the second year of the contract. The school will be hosted by a member of the Working Group. Additional teaching and training activities will take place. For example, ACiD-WG co-operates with the organisation of six-monthly meetings in the UK aimed at PhD students.

Members of the Working Group will engage in activities aimed at generating interest and awareness in asynchronous circuits and systems, e.g., exploratory visits to companies, and tutorials at conferences. They will also disseminate the results of their research, e.g., posters and presentations at conferences, and publication of books and journal articles. Trip reports will be produced and linked to the ACiD-WG website.

To demonstrate the strength of European RTD in asynchronous circuits and systems, participation in the annual "Async" international symposium is particularly desirable.

A report "Design, Automation and Test for Asynchronous Circuits and Systems" will be commissioned, which should be of value to potential users of asynchronous circuit technology and to tools developers. It will be followed up by an annual public overview of the status of asynchronous design in industrial use.

### **Milestone**

There is a single milestone, two years from the start of this four-year contract. The work carried out up to this point will include organisation of

- two workshops (contributing to the systematic exchange of information and the forging of links),
- a summer school (resulting in the training of future designers), and
- an "Async" symposium (facilitating participation by researchers from European industry and academic institutions),

and the production of three reports (informing actual and potential users).

## 2. Membership

MBUK (now known as MBDA) and NNT both signed a membership agreement with SBU during this reporting period. Unfortunately, AT&T closed their research laboratory in Cambridge, terminating their membership. Luciano Lavagno moved from UDI to POLITO, with a consequent change in membership. At the same time FORTH/ICS became a member. The table of members has been updated accordingly:

| <i>Participant No.</i> | <i>Short Name</i> | <i>Country Code</i> | <i>Type of Organisation</i> | <i>Date of entry into force</i> | <i>Date of termination</i> | <i>Requesting Contribution from Commission</i> | <i>Scientific Person</i> |
|------------------------|-------------------|---------------------|-----------------------------|---------------------------------|----------------------------|--|--------------------------|
| 1                      | SBU               | UK                  | U                           | 1/9/00                          |                            | Yes  | Mark Josephs             |
| 2                      | Philips Research  | NL                  | I                           | 1/9/00                          |                            | Yes  | Ad Peeters               |
| 3                      | Infineon          | D                   | I                           | 1/9/00                          |                            | Yes  | Christoph Heer           |
| 4                      | ST                | F                   | I                           | 1/9/00                          |                            | No   | Pascal Vivet             |
| 5                      | CSEM              | S                   | R                           | 1/9/00                          |                            | No   | Christian Piguet         |
| 6                      | IHP               | D                   | R                           | 1/9/00                          |                            | Yes  | Eckhard Grass            |
| 7                      | MBDA              | UK                  | I                           | 19/3/02                         |                            | No   | Eric Campbell            |
| 8                      | UoM               | UK                  | U                           | 1/9/00                          |                            | Yes  | Doug Edwards             |
| 9                      | UNEW              | UK                  | U                           | 1/9/00                          |                            | Yes  | Alex Yakovlev            |
| 10                     | UCAM-CLAB         | UK                  | U                           | 1/9/00                          |                            | Yes  | Simon Moore              |
| 11                     | UPC               | E                   | U                           | 1/9/00                          |                            | Yes  | Jordi Cortadella         |
| 12                     | UDI               | I                   | U                           | 1/9/00                          | 2/5/02                     | Yes  | Luciano Lavagno          |
| 13                     | TUE               | NL                  | U                           | 1/9/00                          |                            | Yes  | Tom Verhoeff             |
| 14                     | INPG-TIMA         | F                   | U                           | 1/9/00                          |                            | Yes  | Marc Renaudin            |
| 15                     | DTU               | DK                  | U                           | 1/9/00                          |                            | Yes  | Jens Sparsø              |
| 16                     | Technion          | IL                  | U                           | 1/9/00                          |                            | Yes  | Ran Ginosar              |
| 17                     | Åbo Akademi       | FIN                 | U                           | 1/9/00                          |                            | Yes  | Kaisa Sere               |
| 18                     | AT&T              | UK                  | I                           | 1/9/00                          | 24/4/02                    | No   | Phil Endecott            |
| 19                     | NNT               | IL                  | I                           | 5/6/02                          |                            | No   | Victor Varshavsky        |
| 20                     | POLITO            | I                   | U                           | 2/5/02                          |                            | Yes  | Luciano Lavagno          |
| 21                     | FORTH/ICS         | EL                  | U                           | 2/5/02                          |                            | Yes  | Christos Sotiriou        |

U = University; R= Research Institute; I=Industrial organisation

SBU has now transferred the advance and first interim payment to all members, with the exception of TUE, which did not supply bank details. Since TUE have once again made a NIL return, with Tom Verhoeff no longer working in the field, TUE's membership will be terminated unless someone suitable is found to replace Tom.

Two more companies became industrial affiliates during this reporting period, namely, MIPS and Sun. The previous contact person at Theseus has left the company, so information is now sent to the Chief Technical Officer. The table of affiliates has been updated accordingly:

| <i>Company Name</i>                                       | <i>Country Code</i> | <i>Home Page URL</i>   | <i>Date of application</i> | <i>Contact Person</i> | <i>Position</i>                |
|---|---------------------|--|----------------------------|-----------------------|--------------------------------|
| Arm Limited   | UK                  | <a href="http://www.arm.com">www.arm.com</a>   | 22/12/00                   | Tim Caspell           | Collaborative Projects Manager |
| Cadence Design Systems                                    | USA                 | <a href="http://www.cadence.com">www.cadence.com</a>   | 24/1/01                    | Ted Vucurevich        | Corporate VP Research          |
| Kramer-Consulting   | D                   | <a href="http://www.kramer-consulting.de">www.kramer-consulting.de</a>   | 6/2/01                     | Torsten Kramer        | Design Engineer                |
| MIPS (Denmark Development Center)                         | DK                  | <a href="http://www.mips.com">www.mips.com</a>   | 16/1/02                    | Peter Jensen          | Design Engineer                |
| Sun Microsystems Laboratories (Asynchronous Design Group) | USA                 | <a href="http://research.sun.com/a_sync">research.sun.com/a_sync</a>   | 6/8/02                     | Jo Ebergen            | Senior Staff Engineer          |
| Theseus Logic   | USA                 | <a href="http://www.theseus.com">www.theseus.com</a>   | 7/2/01                     | Karl Fant             | Chief Technical Officer        |
| Philips Semiconductors Nymegen (Automotive)               | NL                  | <a href="http://www.semiconductors.philips.com/markets/automotive/">www.semiconductors.philips.com/markets/automotive/</a> | 8/2/01                     | Patrick Heuts         | Digital IC Design Engineer     |

### 3. Workplan and Progress

#### 3.1 General description

The three objectives of ACiD-WG can be met by following a workplan that consists of four workpackages:

- WP1 facilitates the systematic exchange and dissemination of information, and the forging of links between members of the Working Group and other parties. By this means,
  - research problems will be articulated and addressed,
  - the potential of applications to benefit from asynchronous circuit technology will be examined,
  - a consensus will build up on design flow, methodology, tools and libraries,
  - plans for standardisation can be formulated, and
  - individual RTD projects (e.g. funded by national research councils) will receive the attention of a wider audience, which should be mutually beneficial.

WP1 is associated with six tasks and four deliverables.

- WP2 is concerned with training measures that promote and support the dissemination, exploitation and enhancement of research knowledge. WP2 is associated with one task and deliverable.
- WP3 produces reports that will help companies assess and evaluate asynchronous design. It is associated with two tasks and six deliverables.
- WP4 is for Project Management. It is associated with five tasks and no deliverables.

### 3.2 Workpackage list

| Workpackage list            |  |                                 |                            |                          |                        |                             |
|-----------------------------|--|---------------------------------|----------------------------|--------------------------|------------------------|-----------------------------|
| Workpackage No <sup>1</sup> | Workpackage title                                    | Lead contractor No <sup>2</sup> | Person-months <sup>3</sup> | Start month <sup>4</sup> | End month <sup>5</sup> | Deliverable No <sup>6</sup> |
| WP1                         | Systematic exchange and dissemination of information | 1                               | 0                          | 0                        | 48                     | D1 - D4                     |
| WP2                         | Training   | 1                               | 0                          | 0                        | 48                     | D5                          |
| WP3                         | Assessment and evaluation                            | 1                               | 0                          | 0                        | 48                     | D6 - D11                    |
| WP4                         | Project management                                   | 1                               | 10                         | 0                        | 48                     |                             |
|                             | <b>TOTAL</b>   |                                 | <b>10</b>                  |                          |                        |                             |

<sup>1</sup> Workpackage number: WP 1 – WP n.

<sup>2</sup> Number of the contractor leading the work in this workpackage.

<sup>3</sup> The total number of person-months allocated to each workpackage.

<sup>4</sup> Relative start date for the work in the specific workpackages, month 0 marking the start of the project, and all other start dates being relative to this start date.

<sup>5</sup> Relative end date, month 0 marking the start of the project, and all end dates being relative to this start date.

<sup>6</sup> Deliverable number: Number for the deliverable(s)/result(s) mentioned in the workpackage: D1 - Dn.

### 3.3 *Workpackage descriptions and progress*

#### Workpackage description

|                                       |   |
|---------------------------------------|---|
| <b>Workpackage number/title :</b>     | 1. Systematic exchange and dissemination of information |
| <b>Start date or starting event:</b>  | 0   |
| <b>Participant number:</b>            | 1   |
| <b>Person-months per participant:</b> | 0   |

#### Objectives

Objectives 1, 2 and 3 are relevant to this workpackage.

#### Description of work

Four workshops will be organised in all, one per year. The workshops will be hosted by members of the Working Group and will take place in different member and associated states of the European Union. Workshops may target specific themes relevant to asynchronous circuits and systems. Attendance and presentations by all members of the Working Group and by industrial affiliates will be encouraged. Invitations to participate will also be extended to non-members of the Working Group. Thirty or more participants are anticipated at each workshop.

In addition, visits between members will take place and special interest group meetings will be organised.

Members of the Working Group will engage in activities aimed at generating interest and awareness in asynchronous circuits and systems, e.g., exploratory visits to companies, and tutorials at conferences. They will also disseminate the results of their research, e.g., posters and presentations at conferences, and publication of books and journal articles.

Trip reports will be produced and linked to the ACiD-WG website.

To demonstrate the strength of European RTD in asynchronous circuits and systems, participation in the annual "Async" international symposium is particularly desirable. ACiD-WG will provide financial sponsorship for Async 2002 and Async 2004.

#### Deliverables

The proceedings of each workshop is a deliverable. They will be published as a technical report of the host institution and will also be made available in electronic form linked to the ACiD-WG website.

#### Tasks and expected result

The organisation of four workshops by members of the Working Group are tasks that will contribute to the systematic exchange and dissemination of information, and the forging of links between members of the Working Group and other participants. The organisation of two "Async" symposia by members of the Working Group are tasks that will facilitate participation by researchers from European industry and academic institutions.

**Progress with Workpackage No. 1:**

**26-28 September 2001.** Two papers (one joint between UPC and Institute of Analytical Instrumentation, Russian Academy of Science, St. Petersburg, and the other by UoM) on asynchronous circuit design were presented at PATMOS, Yverdon-Les-Bains, Switzerland. Heer (Infineon) was invited to discuss low-power circuit design from an industrial perspective.

**1 October 2001.** Heer (Infineon) hosted a meeting with Lavagno (UDI/POLITO), Yakovlev (UNEW), Renaudin (INPG-TIMA), Moore (UCAM-CLAB) and Sotiriou (FORTH/ICS), Munich, Germany, to investigate the feasibility of developing a practically usable design flow for asynchronous circuits, based on standard languages and tools.

**10-12 October 2001.** Renaudin (INPG-TIMA) gave a talk entitled "Asynchronous Systems Design" at the MEDEA+ Conference on "Application-oriented SoC Design: From MEDEA to MEDEA+", Veldhoven, The Netherlands.

**17-18 October 2001.** Renaudin (INPG-TIMA) talked about asynchronous technology and embedded systems at sOc 2001, a two-day seminar on smart devices hosted by France Telecom R&D, Meylan, France.

**12-13 November 2001.** Sparsø (DTU) gave a tutorial on asynchronous circuit design at NORCHIP, Stockholm, Norway.

**December 2001.** Sparsø (DTU) and Furber's (UoM) book "Principles of Asynchronous Circuit Design - A Systems Perspective" was published by Kluwer Academic Publishers. It includes a chapter by Philips Research (and others) describing the results of the design experiment DESCALE (FP4 ESD-LPD contract no. 25519).

**3-5 December 2001.** Renaudin (INPG-TIMA) co-authored a paper in the "timing issues" session of IFIP VLSI-SOC Montpellier, France, as did Heer (Infineon).

**11-18 December 2001.** Smirnov (UPC) visited UNEW for the purpose of collaborative research.

**28-29 January 2002.** Heer (Infineon) hosted the second ACiD-WG workshop, Munich, Germany, with the assistance of Grass (IHP). There were 71 participants, 23 of whom were from industry. 18 members of ACiD-WG were represented, the exceptions being ST, TUE and NNT. The cost of organising the workshop was €8.2K.

The workshop consisted of 26 presentations over 8 sessions:

1. Design Methods/Tools I
2. Design Methods/Tools II
3. Novel Implementation Techniques
4. Poster Introduction and Viewing
5. Design Flows
6. Verification and Test
7. Keynote Speaker
8. Invited Speakers

The poster session was an innovation and worked well. The keynote speech by Furber (Manchester) was a first overview of the status of asynchronous design in industry (Deliverable D8). Handouts of abstracts and slides, together with the methods/tools report (Deliverable D7), were given to attendees and were uploaded on to the ACiD-WG website, to form an electronic version of the proceedings of the workshop (Deliverable D2). An unsuccessful attempt was made to get press coverage, though one or two reporters did attend Sessions 7 and 8, and the presentation of the Methods/Tools Report. At the workshop dinner, there was an opportunity to learn about the operation of a Bavarian microbrewery!

**March 2002.** Cortadella (UPC), Kishinevsky (Intel), Kondratyev (Cadence Design Systems), Lavagno (POLITO) and Yakovlev's (UNEW) book "Logic Synthesis of Asynchronous Controllers and Interfaces" was published by Springer. It describes the theory that underpins their petrify CAD tool.

**4-8 March 2002.** Cortadella (UPC) and Lavagno (POLITO) were Technical Programme Chairs for Synchronisation Methods and for System Design Methods, respectively, at DATE, Paris, France. Lavagno and Renaudin (INPG-TIMA) acted as moderators of the sessions on "Asynchronous Circuits and Clock Scheduling" and "High-Level Synthesis and Asynchronous Pipelines". UoM (joint with Columbia University) and UNEW had papers accepted for the former session.

- 8-11 April 2002.** UoM hosted the Eighth International Symposium on Asynchronous Circuits and Systems (Async '02). There were 118 participants, 21 of whom were from industry. 12 members of ACiD-WG were represented, and they authored 9 of the 21 papers accepted for presentation, as follows: 2× Philips Research (1 joint with KJIST, South Korea, and 1 joint with the University of Twente, The Netherlands), 2× UCAM-CLAB, 1× IHP, 2× UNEW, 1× TUE, 1× UoM. The proceedings were published by the IEEE Computer Society. ACiD-WG, ARM, Fulcrum Microsystems, Intel, Philips Research and Theseus Logic supported the event. ACiD-WG covered attendance by its own members and €1.8K in bursaries for 3 research students (from the Universities of Southampton and Kingston, UK, and the University of Twente, The Netherlands).
- 27-28 May 2002.** Sotiriou (FORTH/ICS) visited POLITO to discuss progress concerning design flows for asynchronous circuits based on standard tools, and to define a possible demonstrator.
- 1 July 2002.** FP5 demonstration contract IST-2002-37796 "Asynchronous Open-Source Processor IP of the DLX Architecture" (ASPIDA) started. It involves ACiD-WG members FORTH/ICS, UoM and POLITO.
- 8-9 July 2002.** A presentation was given in Brussels, Belgium, of the project "Petrify: methodology and tool for logic synthesis of asynchronous circuits" co-ordinated by Cortadella (UPC) in co-operation with Lavagno (POLITO), Yakovlev (UNEW), Kishinevsky (Intel) and Kondratyev (Cadence Design Systems). As a result, the project was selected as one of the ten finalists for the 2002 Descartes Prize. The prize aims to raise awareness of the achievements of European scientists, highlighting the benefits of working together and the importance of the results achieved.
- 27-31 July 2002.** A joint paper between UNEW and the University of Augsburg, Germany, was presented at CAV, Copenhagen, Denmark.

**Workpackage description (continued)**

|                                       |             |
|---------------------------------------|-------------|
| <b>Workpackage number/title :</b>     | 2. Training |
| <b>Start date or starting event:</b>  | 0           |
| <b>Participant number:</b>            | 1           |
| <b>Person-months per participant:</b> | 0           |

**Objectives**

Objective 3 is relevant to this workpackage.

**Description of work**

A summer school will be organised for the second year of the contract. A member of the Working Group will host the school. Lecturers will be drawn from members of the Technical Management Committee and other distinguished scientists. Laboratory sessions will be based on design tools that are available in the public domain.

Additional teaching and training activities will take place. For example, ACiD-WG co-operates with the organisation of six-monthly meetings in the UK aimed at PhD students. ACiD-WG will assist in the placement of suitable PhD students with companies (e.g., summer internships).

**Deliverables**

The lecture notes of the summer school will be collated to form a deliverable.

**Tasks and expected result**

The organisation of the summer school is a task that will result in the training of university students, young researchers and practising engineers in asynchronous circuit design.

**Progress with Workpackage No. 2:**

- 17-18 December 2001.** The 11<sup>th</sup> UK Asynchronous Forum was hosted by UCAM-CLAB, attracting 39 participants. It included a tutorial on "Tracing the behaviour of asynchronous circuits" by Josephs (SBU).
- 7-11 January 2002.** Cortadella (UPC) and Garside (UoM) gave a tutorial on logic design of asynchronous circuits at the ASPDAC and VLSI Design conferences, co-located in Bangalore. Yakovlev (UNEW) helped in the preparation.
- 8 April 2002.** At the tutorial day preceding Async'02 in Manchester, UoM and INPG-TIMA gave tutorials on their CAD tools, Balsa and TAST, respectively.
- 17-18 June 2002.** The 12<sup>th</sup> UK Asynchronous Forum was hosted by SBU, attracting 35 participants.
- 15-19 July 2002.** An ACiD-WG Summer School was hosted by INPG-TIMA, Grenoble, Lecturers included Furber (UoM), Cortadella (UPC), Nowick (Columbia University, New York), Peeters (Philips Research), Josephs (SBU) and Ginosar (Technion). Hands-on tutorials were provided for the CAD tools Petrify (UPC), MINIMALIST (Columbia), Balsa (UoM) and TAST (TIMA). 90 people attended, including lecturers, tutors and helpers. 11 members of ACiD-WG sent students: INPG-TIMA, DTU, ST, IHP, ICS/FORTH, POLITO, UPC, SBU, UCAM-CLAB, UoM, UNEW. Students received lecture notes and tutorial material (Deliverable D5) and a copy of Sparsø and Furber's textbook "Principles of Asynchronous Circuit Design - A Systems Perspective". The availability of the second overview of the status of asynchronous design in industry (Deliverable D9) was announced.
- 12-14 August 2002.** Oklobdzija (U.C. Davis) and Sparsø (DTU) gave an embedded tutorial entitled "Future Directions in Clocking Multi-Ghz Systems" at ISLPED'02, Monterey, California. They explained clocking and skew tolerant flip-flops, and presented asynchronous circuit design as an alternative when one cannot control timing precisely. Piguet (CSEM) was programme co-chair.
- 26-30 August 2002.** Heer (Infineon) and Piguet (CSEM) were instructors on the EuroPractice Advanced Digital IC Design course, EPFL - Lausanne, Switzerland. They taught "Asynchronous Design Methods" and "Low-Power Systems on Chip", respectively.

**Workpackage description (continued)**

|                                       |                              |
|---------------------------------------|------------------------------|
| <b>Workpackage number/title :</b>     | 3. Assessment and evaluation |
| <b>Start date or starting event:</b>  | 0                            |
| <b>Participant number:</b>            | 1                            |
| <b>Person-months per participant:</b> | 0                            |

**Objectives**

Objectives 2 and 3 are relevant to this workpackage.

**Description of work**

The Working Group will commission a report "Design, Automation and Test for Asynchronous Circuits and Systems" which will describe the state-of-the-art in methods and tools for the design of asynchronous digital VLSI systems. The report is intended to be primarily of use to companies (members and non-members of the Working Group alike) who are aware of the potential benefits of asynchronous circuit technology, but who need to know more about available asynchronous design methods and tools before committing resources. The report will also highlight deficiencies in existing approaches and so provide the impetus for further tool development.

The Working Group will also produce an annual public overview of the status of asynchronous design in industry, including an update on tools.

**Deliverables**

Preliminary and final versions of the commissioned report will be delivered. The latter will be made available in electronic form on the world wide web during the first year of the contract. A report will be delivered at the end of each year of the contract to provide an overview of the status of industrial-design. Again, these will be made available on the web.

**Tasks and expected result**

The TMC will undertake the task of reviewing the preliminary version of the commissioned report and providing feedback to the author within one month of delivery. Members and industrial affiliates will have the task of contributing to the annual overview.

**Progress with Workpackage No. 3:**

**3 January 2002.** Manchester Informatics produced a version (labelled 1.3) of the report "Design, Automation and Test for Asynchronous Circuits and Systems" (Deliverable D7). This was printed by Infineon and distributed at the ACiD-WG workshop, 28-29 January, as mentioned under Workpackage No.1. It is available from the ACiD-WG website.

**27 June 2002.** Manchester Informatics produced a version (labelled 1.1) of the report "The Status of Asynchronous Design in Industry" following feedback from the Project Manager. It was agreed that this would be treated as Deliverable D9, with Furber's slides from the ACiD-WG workshop being treated as Deliverable D8, as mentioned under Workpackage No.1. It is available from the ACiD-WG website.

**23 July 2002.** Manchester Informatics agreed with the Project Manager to update the reports in time for the next ACiD-WG workshop in January 2003. This would form Deliverable D10.

**Workpackage description (continued)**

|                                       |                       |
|---------------------------------------|-----------------------|
| <b>Workpackage number/title :</b>     | 4. Project management |
| <b>Start date or starting event:</b>  | 0                     |
| <b>Participant number:</b>            | 1                     |
| <b>Person-months per participant:</b> | 10                    |

**Objectives**

This workpackage is concerned with project management.

**Description of work**

N/A

**Deliverables**

N/A

**Tasks and expected result**

The four progress reports are tasks. They will be made available in electronic form on the world wide web at the end of each year of the contract. Another task is to communicate news on a more regular basis. An e-mail distribution list will be maintained for this purpose and web pages will be kept up-to-date.

**Progress with Workpackage No. 4:**

The TMC met once during this reporting period:

**29 January 2002.** The meeting took place following the close of the second ACiD-WG workshop. SBU, POLITO, DTU, Philips Research, Infineon, UoM, MBDA, ICS/FORTH, UCAM-CLAB, UPC, UNEW, Technion, Abo Akademi, IHP and INPG-TIMA were represented. Heer took minutes. Most of the discussion concerned the programme of the summer school. It was agreed that ICS/FORTH would host the third ACiD-WG workshop early 2003 and Abo Akademi would host the final workshop mid 2004.

Other business of the TMC was carried out by electronic mail.

### 3.4 Deliverables list and status

#### Deliverables list

| Del. no. | Deliverable name  | WP no. | Lead participant | Estimated person-months | Del. type* | Security**         | Delivery (proj. month) |
|----------|---|--------|------------------|-------------------------|------------|--------------------|------------------------|
| D1       | Proceedings of 1 <sup>st</sup> workshop                                   | WP1    | 1                | 0                       | Report     | Pub.               | 12                     |
| D2       | Proceedings of 2 <sup>nd</sup> workshop                                   | WP1    | 1                | 0                       | Report     | Pub.               | 24                     |
| D3       | Proceedings of 3 <sup>rd</sup> workshop                                   | WP1    | 1                | 0                       | Report     | Pub.               | 36                     |
| D4       | Proceedings of 4 <sup>th</sup> workshop                                   | WP1    | 1                | 0                       | Report     | Pub.               | 48                     |
| D5       | Lecture notes from summer school  | WP2    | 1                | 0                       | Report     | Rest. <sup>1</sup> | 24                     |
| D6       | Preliminary version of commissioned report on design, automation and test | WP3    | 1                | 0                       | Report     | Int.               | 6                      |
| D7       | Final version of commissioned report                                      | WP3    | 1                | 0                       | Report     | Pub.               | 10                     |
| D8       | 1 <sup>st</sup> overview of status of asynchronous design in industry     | WP3    | 1                | 0                       | Report     | Pub.               | 12                     |
| D9       | 2 <sup>nd</sup> overview  | WP3    | 1                | 0                       | Report     | Pub.               | 24                     |
| D10      | 3 <sup>rd</sup> overview  | WP3    | 1                | 0                       | Report     | Pub.               | 36                     |
| D11      | 4 <sup>th</sup> overview  | WP3    | 1                | 0                       | Report     | Pub.               | 48                     |

\* A short, self-evident description e.g. report, demonstration, conference, specification, prototype...

\*\*Int. Internal circulation within project (and Commission Project Officer if requested)

Rest. Restricted circulation list (specify in footnote) and Commission PO only

IST Circulation within IST Programme participants

FP5 Circulation within Framework Programme participants

Pub. Public document

<sup>1</sup> To include attendees at the summer school, and ACiD-WG members and industrial affiliates.

#### Status of deliverables:

All deliverables scheduled for the first and second reporting periods have now been delivered, namely, D1-D2 and D5-D9.

