Session 5

SWOT: Strengths, Weaknesses, Opportunities, Threats

- System integration
- Design automation
- Robustness
- Power
- Performance
Session 5

SWOT : Strengths, Weaknesses, Opportunities, Threats

- System integration 5
- Design automation 4
- Robustness 2
- Power 1
- Performance 1

--

13 / 37 attendees
Session 5

SWOT : Strengths, Weaknesses, Opportunities, Threats

- System integration 5 Frank Gurkaynak
- Design automation 4 Jens Sparsoe
- Meeting design constraints 4 Ran Ginosar

12-14 people per group
Session 5

SWOT: Strengths, Weaknesses, Opportunities, Threats

- 45 minutes brainstorming
- 10 minutes break
- 30 minutes reporting

Objectives
- For each topic establish SWOT lists and justify
- Good/bad for … because …
- Modulate according to contexts, types of asynch. circuits …
- Status, recommendations, propositions …
Session 5

System integration (functional, logical, physical)

Synchronization (GALS, GALA, NoC…)
IP procurements, validation …
Reuse, Migration
Interfaces (VSIA…)
Top Level P&R, Signal integrity/buffering

Properties : Modularity, locality, reliability…
Session 5

Design automation

Specification languages
Verification
Logic synthesis
ATPG
Gate level verification, equivalence…
P&R
STA
Std cells, Full Custom, Hybrid…
Session 5

Meeting design constraints

Area
Speed
Power
Security
Robustness
Testability …
Session 5

12-14 people per group

System integration (Frank) : room Regina 5

Design automation (Jens) : room Regina 6

Meeting design constraints (Ran) : this room
SWOT

• Strengths
• Weaknesses
• Opportunities
• Threats
Design automation : Strengths

• Specification languages
  – Separation of computation and communication

• Tools
  – Behavioral synthesis
  – DI and Submicron
  – Model checking applicable to async. Circuits
  – Synthesis exists
  – Less constraints on P&R
  – Std cell libraries can be used
Design automation : Weaknesses

• Specification languages
  – Non standard languages
  – Small group, lack of aggression

• Tools
  – P&R constraints of existing tools related to clk
  – Static timing analysis is specific
  – Behavioral synthesis is just starting
Design automation: Opportunities

• Specification languages
  – Specify appropriate languages within coming system level specification languages
  – Interface abstraction (VSIA)
  – Training

• Tools
  – Density, locality => tools are simpler
  – Should/need to adapt/modify existing tools
  – Behavioral synthesis is not cycle true
  – Incremental design commercialization
Design automation: Threats

• Specification languages
  – Async misses opportunities

• Tools
  – Developing good asynchronous tools may take too long
System integration: Strengths

- Clock-tree reduction
- Fewer synchronisation points
- Lower EMI in the system
- Modularity
- System complexity better scalable
- Independence of robustness and performance
- Reliable global communication
- Peak power reduction
- Automated power management (Automated voltage scaling)
- Supports diverse environment (mixed-signal, etc.)
System integration : Weaknesses

• Verification
• Production testing
• Lack of commercial tools
• Lack of experience in industries
• Lack of standards (interfaces, libraries, performance measurements)
• Prototyping hardware not available (FPGA, etc.)
• Less predictable for real-time problems
• All ATE is synchronous
System integration : Opportunities

- Infinite scalability
- Smart cards and crypto products
- Market for new tools
- More diversity, configurable
- Compatibility with emerging technologies (token based computing, dataflow, distributed control, single electron transistor …)
- Platform design
System integration : Threats

• Industry (resistance to new ideas)
• Legacy
• Investment in clocked design
• “Asynchronous illiteracy”
• Short term planning due to market pressure, time-to-market
• Critical mass will not be reached if results are not forthcoming
• Lack of joint effort
Meeting design constraints : Strengths

• Area:
  – No clock trees,
  – (sometimes) more local interconnect

• Power:
  – Dissipated only by active components
  – Dynamic Voltage Scaling – ET2 vs. ET
  – Easier than clock gating

• Speed:
  – Some very fast ckt reported
  – Fast recovery from sleep mode

• Security:
  – Eliminating ref signal / clocks
  – Ckt level security protocols

• Robustness:
  – Higher yield (speed rating)
  – Insensitive to PVT delay variations
  – Less sensitive to EMI

• Testability:
  – Has inherent redundancy (yet to be exploited)

• EMI / Noise:
  – Lower noise—spread transitions
  – EMI controllable by protocols
Meeting design constraints: Weaknesses

- Area:
  - (Sometimes) larger
- Power:
  - Sometimes larger
- Speed:
  - Harder to predict / promise / verify (data dependency)
  - Maybe lower speed due to larger area
- Security:
  - Low power \( \rightarrow \) bad security?
- Robustness:
  - Sensitive to glitches
- Testability:
  - Hard
  - Timing and logic behavior are intermingled
- EMI / Noise:
  - Cannot tune to avoid a certain freq band
Meeting design constraints : Opportunities

- **Area:**
  - Mixed signal (digital functionality in an analog chip)

- **Power:**
  - Sensors

- **Speed:**
  - Deep pipelining for streaming

- **Security:**
  - Smart cards

- **Robustness:**
  - Battery op, portable
  - Automotive (EMI insensitive, voltage drop insensitive)
  - Non-silicon devices (polymer transistors, textile, organic,…)

- **Testability:**

- **EMI / Noise:**
  - Radio RCV
Meeting design constraints: Threats

- Area:
  - Low cost chips
- Power:
  - Clock gating could be just as good??
  - Leakage due to larger area
  - If leakage dominates, sync/async becomes irrelevant
- Speed:
  - May run too fast
- Security:
  - New side channels (info leaks)
- Robustness:
  - Deadlock due to noise
- Testability:
  - No chance without it
- EMI / Noise:
Meeting design constraints : Recommendations

- Not all async methods are created equal
  - Generalizations are useless…
- DFT is most critical challenge