Model of Multi-Level Delay-Insensitive Implementation with Intermediate Signaling

Igor Lemberski, Kiseon Kim

Gwangju Institute of Science and Technology
Department of Information and Communications

E-mail: {lembersk, kskim}@gist.ac.kr
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Introduction

Delay – insensitive (DI) implementation is becoming more and more attractive for designers because correct behaviour of such schematic doesn’t depend on:

- logic elements and wiring delays;
- timing interval the input signal switches its value;
- number of inputs switching their value.

As a result:

- DI schematic is robust and reliable;
- designer doesn’t need to perform timing verification
Seitz’s model

weak conditions

strong conditions

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Composition model

\[ X \langle x_1 \cdots x_n \rangle \rightarrow f_1 \cdots f_n \rightarrow F \quad \text{information} \]

\[ \quad \rightarrow S \quad \text{signalling} \]

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Two-Level (C-OR) Implementation
## Experimental Results

<table>
<thead>
<tr>
<th>Examples</th>
<th>Anantharaman’s implementation</th>
<th>Our implementation</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND(2)</td>
<td>18 x G(2)</td>
<td>10 x G(2)</td>
<td>1.8 times</td>
</tr>
<tr>
<td>AND (3)</td>
<td>102 x G(2)</td>
<td>28 x G(2)</td>
<td>3.64 times</td>
</tr>
<tr>
<td>AND (4)</td>
<td>206 x G(2)</td>
<td>50 x G(2)</td>
<td>4.12 times</td>
</tr>
</tbody>
</table>
Multi-Level DI Implementation(1)

- Shannon decomposition of n variables is applied:

\[
f = x_{i1}x_{i2}\ldots x_{in} F_1(x_{in+1}, x_{in+2}, \ldots x_k) \lor \\
\lor x_{i1}x_{i2}\ldots x'_{in} F_2(x_{in+1}, x_{in+2}, \ldots x_k) \lor \ldots \\
\lor x'_{i1}x'_{i2}\ldots x'_{in} F_2^n (x_{in+1}, x_{in+2}, \ldots x_k)
\]
Multi-Level DI Implementation (2)
Example
Assumption

- Once output \( f(1) \) is in the defined state (it means, sub-function \( F_1 \) is already in state 1) - sub-function \( F_2 \) is in the state 1.

- This assumption is quite realistic. At the time the output becomes defined the signal has propagated through the longest path (form inputs to output). The path that causes switching on sub-function \( F_2 \) is shorter.

- Since we don’t expect huge delay asymmetry for different paths it is reasonable to assume that by the time the output function changes its state to defined one sub-function \( F_2 \) is already in state 1.
Multi-level implementation without signaling at intermediate level:

\[ \forall (F_i, F_j), i \neq j : F_i = F_j \text{ or } F_i \text{ or } F_j, F_i, F_j \in F - \text{set of sub-functions.} \]

In example below: (F1 = F4) or (F2 = F3)

![Diagram with logic gates and inputs](image)
## Experimental Results

<table>
<thead>
<tr>
<th>Example</th>
<th>Two-level</th>
<th>Multi-level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Schm/Sign</td>
<td>Total</td>
</tr>
<tr>
<td>AND(2)</td>
<td>9/6 G(2)</td>
<td>15G(2)</td>
</tr>
<tr>
<td>AND(3)</td>
<td>22/11G(2)</td>
<td>33G(2)</td>
</tr>
<tr>
<td>AND(4)</td>
<td>39/16G(2)</td>
<td>55G(2)</td>
</tr>
</tbody>
</table>

Schm - schematic
Sign - signaling
Conclusion

- For multi-level DI implementation, composition model was proposed.
- Signaling schematic was developed.
- Conditions for multi-level DI implementation without intermediate signaling were formulated.
- Experimental results showed that although complexity of signaling schematic is high the total implementation complexity is almost the same as for two-level implementation due to more simple functional schematic.

Ref.:
I. Lemberski, M. Josephs,