GALS Baseband Processor for WLAN

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Abstract

Current trends in System on Chip (SoC) integration impose a number of technical challenges on designers and tools. In the area of wireless communication systems, the number of difficulties for mixed-signal implementations additionally grows. There is a growing demand for elegant solutions for decreasing power consumption, reducing electromagnetic interference (EMI) between analog and digital circuit blocks, and effective clocking schemes for complex digital systems. Many proposals have been published, but the question which of them will be applied in industrial practice is without answer, yet.

GALS techniques are deployed to solve some problems of SoC integration. There are many different proposals how to create a stable and efficient GALS system. Usually, a GALS system consists of a number of locally synchronous blocks surrounded with asynchronous wrappers. Communication between synchronous blocks is performed indirectly via asynchronous wrappers. The current level of GALS development offers a relatively stable framework for the implementation of complex digital systems. However, known GALS techniques may introduce some drawbacks in performance, additional constraints in the system and hardware overhead. On the other hand, all proposed GALS techniques are oriented towards some general architecture with sporadic and not too intensive data transfer on its interfaces.

We have recently introduced a new request-driven GALS technique, optimized for a datapath architecture with bursty, but very intensive data transfer. We decided that after GALSification of relatively small experimental designs, the complete spectrum of advantages and disadvantages of our proposed request-driven GALS technique could be investigated best in a typical complex datapath application. Our activity to work in the GALS area was initiated with the development of an IEEE 802.11a compliant modem. The baseband processor for that standard appears to be a perfect candidate for introducing GALS. It is a relatively complex design (around 700k gates) with an internal datapath structure, which includes sub-blocks like Viterbi decoder, FFT/IFFT processor, and different CORDIC processors. Introducing the GALS mechanisms in this baseband processor was a real challenge and some results of this work will be reported here. Details of the GALS partitioning and some additionally developed blocks will be discussed. Furthermore, the design-flow, implementation results and power estimation numbers are reported.