The automated design of an asynchronous DLX microprocessor will be presented. The microprocessor has been designed beginning with a standard RTL-like Verilog specification and the Pipefitter design flow has been used to automatically generate both the specification for the direct implementation of the Control Unit and a synthesisable Verilog specification of the Data Path. The architecture of the DLX is locally synchronous and globally asynchronous (bundled data) and the delay elements for the generation of the local clock signal are automatically produced by Pipefitter as well. Synchronization is achieved by means of a four-phase protocol.

All the steps of the design flows (i.e., logic synthesis, technology mapping, placement and routing) have been completed using standard tools leading to the layout of the circuit.

The final microprocessor implements all the functionalities of a standard DLX (with the exception of the floating point unit) and supports its whole set of instructions.

Some considerations on the area occupation of the microcontroller will be also presented.