Abstract:

We present an asynchronous version of the DLX processor, obtained by using the "de-synchronization" approach, which replaces the clock distribution tree of a traditional synchronous circuit by a local synchronization mechanism.

We first implemented the conventional synchronous DLX architecture in synthesizable Verilog RTL code. Then, based on this synchronous implementation, we obtained an asynchronous version of the DLX processor by applying the method of de-synchronization. We replaced the clock tree by asynchronous driving logic (implemented using simple asynchronous controllers) and introduced handshaking into the datapath, wherever synchronization between data and instructions was necessary (e.g. for data forwarding).

We present a comparison between our model, an automatically synthesized DLX based on the Pipefitter design flow, and the conventional synchronous reference design.