Optimizing Scan Test for Asynchronous Circuits

ACiD-WG Workshop

Frank te Beest

Outline

♦ Motivation
♦ Full Scan Overview
♦ Three Scan Optimizations
♦ Results
♦ Planning
♦ Conclusions
Goal

- Automated structural test method for asynchronous circuits designed with the Tangram toolset

How

- Add a synchronous test mode to the circuit
- Apply conventional test tools
- Focus on similarities, work around differences

Motivation

- Three criteria for test methods:
  - Quality: Fault coverage
  - Effort: Development time
  - Cost: Area / Pin overhead, Test time
- The increasing importance of High Quality and Low Effort, make scan test attractive despite the high area overhead
- Area overhead can be reduced significantly by various optimizations
Full Scan

♦ All state holding (memory) elements need:
  – to be controlled by an external clock
  – to be part of a serial scan chain
♦ Remaining logic should be:
  – free of (combinational) loops
  – non-redundant

Tangram circuit structure
Data path

Control Part
Scan C-elements

Implemented with standard cells

Test conflict

Clock signals

Data signals

PHILIPS
Test flow

Test vectors

ATPG

design_control.v

design_data.v

design_scan.v

design_control.pat

design_data.pat

Test vectors

ADPROM

DES

TODONIA

&8c1

Average

Full Scan, standard library

Average area overhead (%)

Full Scan, standard library

Average area overhead (%)

Control part

Data path
Optimizations

Three possible optimizations, to reduce the large DfT-area are:

- Custom cells for scan C-elements
- L1L2 scan
- Partial scan

Custom scan C-elements

Uses half the area of the standard cell implementations
Full Scan, custom cells (Est.)

Average area overhead (%)

L1L2 scan
LIL2 scan

Graph problem:
- Vertices: Latches and Flip-Flops
- Edges: Connections between Latches and Flip-Flops

Find a 2-coloring of a graph:
- with minimal conflicts
- where both colors are of equal size
- all latches / flip-flops corresponding to a latch controller have the same color.

Full scan, LIL2 data path (Est.)

![Graph showing average area overhead (%)](image-url)
Partial scan

C-element ACZ:

Truth table

<table>
<thead>
<tr>
<th>B</th>
<th>A</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
<td>0</td>
<td>Z</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
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</tbody>
</table>

3 out of 4 input combinations have combinational effect
Only 1 combination is state holding

Test for s_a_1 on ::

a: 0 0
b: 0 1

Test for s_a_0 on ::

a: 1 0
b: 1 1
Partial scan

To test a circuit containing unscanned C-elements with 2 test patterns, the pins of the C-element have to be combinationally and hazard free controllable and observable.

Test independent C-elements

Relates to “independent set” problem from graph theory

Simple heuristic algorithm implemented: ±25 % reduction of scan elements in the control part.
Conclusions

- Tangram circuits can be scan tested with a high fault coverage
- <30% area overhead is achievable with
  - Custom cell implementation of Scan C-elements
  - L1 L2 scan (in data path)
  - Partial scan (in control block)
- Further optimizations leading to 20 – 25% overhead
  - Better algorithms
  - Apply L1L2 and partial scan over the entire circuit
  - Writing for Testability