Multi-point Interconnect for Globally-Asynchronous Locally-Synchronous Systems

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Globally-asynchronous locally-synchronous (GALS) operation employs a self-timed communication scheme on a coarse grained block level and combines the following features:

- All major modules are designed in accordance to proven synchronous clocking disciplines.
- Data exchange between any two modules strictly follows a full handshake protocol.
- Each module is allowed to run from its own local clock.
- Any asynchronous circuitry necessary for coordinating the clock-driven with the self-timed operation is confined to “self-timed wrappers” arranged around each clock domain.

GALS makes it possible to take advantage of the industry-standard synchronous design methodology within individual clock domains and of self-timed operation across clock boundaries. The self-timed approach does away with the need to time-align the operation of all modules within the framework of a common base clock period. Instead, each module is driven from a local pausable clock generator in its self-timed wrapper being controlled such as to prevent any timing violations from occurring within the Locally Synchronous Island’s data interface.

Fig. 1 depicts a block level schematic of a GALS module with its self-timed wrapper surrounding the locally synchronous island. The wrapper contains an arbitrary number of GALS ports, a local pausable clock generator, and test structures.

GALS bus: A shared bus solution as shown in fig. 2 is obtained from extending the port controllers that manage the self-timed data transfers between different GALS modules. The ability of proper arbitration for the shared bus resources is added in order to support multiple transmitters and receivers. Arbitration as well as address decoding will be central for sake of area and power efficiency. This has no great impact on the modularity as the final structure has to be fixed at the time of synthesis.

Ring structure: In a ring topology, all nodes are connected with a circular path. At each node local address decoders decide whether a received data word is bound for itself or is to be passed on to the successor node. Every node can also insert new data into the ring.

Figure 1: GALS Module with Locally Synchronous Island surrounded by the Self-Timed Wrapper

Figure 2: GALS bus
Such a ring can be constructed from existing GALS modules connected with point-to-point links. However, dedicated self-timed GALS ring transceivers seem more appropriate to decouple the synchronous island from the ring’s timing and to unburden it from time consuming re-routing tasks (fig. 3). The associated host circuitry within a island is then attached to the transceiver with a point-to-point connection.

Arbitration is performed in the transceivers (distributed arbitration). An arbiter element decides which request to pass (incoming request from the preceding ring transceiver, or request from the host circuitry that wants to feed a data packet into the ring). Therefore, this approach is modular and easily scalable. No central instance is necessary and no distinction is made between masters and slaves. Because the packets have to pass other transceivers before reaching their destination, the latency is higher compared to the GALS bus. On the other hand the reduction of the length of the connecting wires scales down wire capacitance and crosstalk effects and thus higher throughput is expected.

Figure 3: Ring structure

We are currently working towards a new test implementation that includes improved clock generators with refined tunability, advanced test structures, and the aforementioned interconnection topologies. The measurement and test results of this chip will provide us with more profound knowledge in building GALS systems and allow a direct comparison of different clock generators and interconnection approaches.