Asynchronous CORDIC implementation

B. Sarker, E. Grass, K. Maharatna

IHP
Im Technologiepark 25
15236 Frankfurt (Oder)
Germany

CORDIC : Implementation

Three CORDIC processors were implemented, viz.,

• Asynchronous -
  1. Using master slave D Flipflop as data buffers (ASY-dff CORDIC)
  2. Using latches as data buffers (ASY-latch CORDIC)

• Dual mode -
  It can operate in both synchronous as well as asynchronous mode of operation with a mode signal which allows the design to switch between the synchronous and asynchronous mode.
Layout of Dual Mode CORDIC

- Total core area after layout = 2.6 mm²
- Total number of digital pins = 67
- Frequency of operation = 45 MHz (simulated)
- Total gate count = 43 k invertors
- Designed with pads on three sides and analogue circuits on the east side of the layout for crosstalk measurements.

Implication and future plan

- The latency in the asynchronous mode of operation is smaller compared to synchronous operation.
- The dual mode CORDIC had an area overhead of 13% compared to the synchronous version.
- Area of the latch based is smaller than the D Flipflop based CORDIC.
- Dual mode operation gives the option to have both the advantages of asynchronous as well as synchronous operation, as this gives an optimal compromise to reduce crosstalk, power dissipation, throughput and latency.

Future plan

- The Dual mode CORDIC design has been taped out for fabrication using IHP in-house 0.25 µm SiGe:C BiCMOS technology.
- Noise measurements are planned in March 2002.