As far as very deep sub-micron SOC design is concerned, integrated analog and RF parts on chip induce EMI noise through strong current variations.

It has been proved that asynchronous circuits provide an efficient means of reducing current variations when compared to synchronous ones.

Given this context, we proceed in two steps. On the one hand, we determine and quantify the current activity in different kinds of asynchronous circuits: micropipeline, QDI, both using different communication protocols. On the other hand, we shape the current consumption of asynchronous circuits by controlling internal delays and optimizing the gate logical structures.

In this presentation, the methodology and the design flow used to design an asynchronous micropipeline circuit are briefly presented. Then, delay tuning impact on the asynchronous circuit current profile is demonstrated.

The work is based on electrical simulations performed on an asynchronous FIR (Finite Impulse Response) filter. The current consumption is analyzed block per block to get a current model for each circuit part. Then, these models are used to elaborate a design methodology to shape the circuit current profile. This methodology is based on the delay scheduling inside the whole circuit control part.

It is shown that the experimentation performed validates the approach and enables us to envision automated current shaping. The ultimate goal is to integrate this method in our TAST synthesis tool.