On-chip test for timing conditions

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With the reduction in dimensions and consequent increasing speed of digital circuits, sub-micron devices show increasing variability of delays. Parametric changes, as well as spot defects, may cause the dynamic behavior of a circuit to change, resulting in timing problems. Fully asynchronous, and delay insensitive methods can be used to ensure functional correctness, but do not always produce high performance, and fully synchronous or globally asynchronous, locally synchronous systems (GALS) which rely on fixed clocks and use pre-existing libraries of synchronous cells are often preferred. While these systems can be fully tested functionally by adding test structures on chip, timing issues remain a problem, particularly the timing margins available when working at full speed, and the need to ensure set-up and hold times for the input output interfaces. The first problem requires a tester that is able to vary the clock frequencies by small increments and supply data patterns at full speed, and the second problem also requires the tester to adjust data and clock to very accurate absolute timing margins, perhaps as low as 20ps.

All systems on chip must be interfaced to off-chip inputs and outputs, and consequently these interfaces must be tested to absolute timing margins for parameters such as set-up and hold times. Testing I/O parameters at high-speed and/or accuracies of better than 100ps involves very high-performance automatic test equipment, and the cost of such testers is becoming prohibitive ($600k for a development tester; $4M for a production tester). Current trends in on chip complexity and internal bandwidth, compared to the bandwidth available for external test suggest that the ratio of internal to external bandwidth will increase by over an order of magnitude from 5.4:1 in 2002 to 94:1 in 2011, making the use of built in test methods essential. Current trends are narrowing the difference between the period of the device under test, and the timing accuracy of the signals from any external tester. This problem could lead to an unacceptable reduction in device yield, since uncertainty in test accuracy leads to device rejection. The ratio between device period and tester accuracy, currently around 5:1 in 2002, is likely to move towards 2.5:1 in 2011, because it is difficult to time external inputs to much better than 100ps, a physical distance of less than 30mm.

We describe techniques that allow the design of digitally set delay lines with accuracy better than 8ps. When used in conjunction with MUTEX time comparison, and time amplification circuits it is possible to measure on-chip signal path timing differences to accuracies of better than 10ps. This accuracy is currently mainly limited by the effects of fabrication imperfections in the MUTEX circuits that have been modelled in an 0.6µ CMOS technology. Processes with smaller dimensions may allow this figure to be reduced to less than 5ps, because the MUTEX circuits and inverters will be faster, but further reductions are likely to be dependent on careful interconnect layout, which will then dominate the delay setting accuracy. These time measurement methods can be used in delay fault testing and in input tests, such as data set-up time conditions. We describe an on-chip method of testing these conditions, which may take its inputs from the chip boundaries in the same way as the external tester, but instead of using expensive, accurate external signal sources, we use uncorrelated signals whose statistics are known, and accurately select the conditions to be tested on-chip.