Mission Statement

“To be the world’s leading supplier of self-timed solutions for system-on-chip applications”

Why Self-Timed?

◆ Competitive advantages for end-user products

◆ Technology advantages for IP developers
Product Competitive Advantages

- Inherent low power properties
  - data driven: no activity → no dissipation
  - no clock gating required
- Simple power management
  - instant start/stop
  - no software management required
- Low EMI
  - uncorrelated activity: no clock harmonics

Smartcard security
- self-timed circuit technology resists attacks on smartcards
  - analysis of power signature more difficult
  - clock glitch attacks eliminated
  - supply voltage variation attacks reduced
Demonstrators: Low-Power

<table>
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<th>Self-timed Device</th>
<th>Power Improvement</th>
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<td>Philips DCC decoder</td>
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<td>Philips 80C51 clone</td>
<td>×4</td>
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<tr>
<td>Intel P2 instruction length decoder</td>
<td>×2</td>
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Demonstrators: Power Management

- AT&T Research Labs Piconet project
  - Bluetooth precursor
  - AMULET2e used in low-cost wireless networking nodes
  - instant halt/start-on-interrupt simplified system design
  - enabled low cost system with long battery life
Demonstrators: Low EMI

- Philips: self-timed 80C51 in Myna pager
  - microcontroller runs at same time as radio
  - not possible with clocked design
  - 3 pager standards in software
  - single hardware design
- Hagenuk: AMULET3i core of DECT base station
  - chosen because of low EMI properties

Amulet3 EMI

- ARM9
- Amulet3
Smartcard Security: Power Signatures

Conventional clocked design

Dual rail clocked design

Self-timed design

Peaks betray number of 1’s in data word

Technology Advantages for IP Developers

- Complex clock tree design eliminated
- Modularity
  - object oriented hardware design
  - robust delay-insensitive interfaces
  + CHAIN self-timed bus technology
  = simple integration of IP cores
  - GALS (Globally Asynchronous, Locally Synchronous) accommodated
- safety route for conventional designers
Technology Advantages for IP Developers

- Rapid time to market with the Balsa synthesis system
  - e.g. AMULET3i DMA controller
    - complex requirements
    - changing specification tracked
    - three man-months to layout
  - variety of back-ends/protocols available
  - trade area for timing verification effort

Balsa Synthesis Example

- SPA – ARM v5 compatible processor core
  - Designed entirely in Balsa
  - Design time 18 man-months (Amulet3 96 man-months)
  - Process independent
  - Readily customisable
Technology Credibility

- Specialist self-timed companies
  Theseus Logic, ADD, Cambridge spin-off
- Product suppliers
  — Philips
- Other significant industry activity
  — Sun, Motorola (STAR-8), Intel

Company Background

- Formed from the Amulet group at Manchester University:
  — Amulet founded 1990 by Prof. S. Furber, co-architect of the ARM processor
  — recognised world leader in self-timed technology
  — proven chip design skills
Self-timed ARM designs:

- **AMULET1 (1993):**
  - 58k transistors, 25mm² (1μ)

- **AMULET2e (1996):**
  - 450k transistors 25mm² (0.5μ)

- **AMULET3i (2000):**
  - 805k transistors 25mm² (0.35μ)

**Founders’ Track Record**

- **STAVE:** self-timed Viterbi decoder
- **CADRE:** self-timed low-power DSP
- **CHAIN:** on-chip self-timed bus interconnect technology
- **Balsa:** automatic synthesis system for self-timed circuits
Founders’ Track Record

Credibility:

There are only three groups outside ARM sanctioned to design ARM cores:

- Intel
- Motorola
- Amulet

Example Designs
Summary

◆ Product competitive advantages
  low power, simple power management
  —low EMI, smartcard security
◆ Technology advantages
  —modularity, natural tP integration
  —synthesis, time to market
◆ Founder credibility
  —proven track record