The Application of NULL Convention Logic to Commercial Products

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Overview

- Our business approach is based on selling IP and we are seeding the market with ASICs

- We have product silicon.

- We have a working design methodology and tool set that follow standard design flows. We are now optimizing the methodology and tools.

- We have left the R&D phase and are actively pursuing commercial products.
**Theseus Products**

- **Licenses** for NULL Convention Logic. Theseus patented methodology for the design and manufacture of semiconductor chips.
  - Methodology and Tools
  - IP Blocks/macrocells
  - Cell Libraries
  - Training
  - NRE

- **ASICs** for selected high value markets
  - Embedded Medical
  - NCL microcontrollers
  - Smart Cards
  - Base Stations
  - Data Conversion

**Targeted Markets**

- **Total Addressable Market for NCL Technology - $95B**
- **Cost effective systems-on-a-chip**

- Embedded Medical ~ $250M
- NCL08 Micro-controller ~ $1.3B
- Smart Card Chips ~ $2B
- Base Station IC's ~ $1.2B
- Data Conversion ~ $1.5B
- Other Markets

- Partnering with customers in high growth markets with high-value NCL products
**Embedded Medical**
- First product complete - wavelet coprocessor
- Strategic Alliance with Medtronic - $1M plus 3% royalty
- Medtronic number one company in this market with 80% share
- Strategic Equity investment by Medtronic. Product insertion scheduled for May 2002

**NCL 08 Micro-controllers**
- Micro-controller product exceeded performance goals set by Motorola.
- Metroworks (Motorola division) and P&E Microelectronics committed to providing user support.
- Motorola VP supporting product insertion.
- Demonstration Boards delivered to 4 customers. First sales anticipated by mid 2002.
- Strategic equity investment by Motorola

**Smart Card**
- Infineon purchased design license. Encryption chip in fabrication.
- We have designed an asynchronous RSA encryption engine
- In discussion with strategic investors

**Base Transceiver Station**
- MathStar bought NCL design license. Started design of high speed NCL filter chip
- Interpolating DAC product specification defined.
- First user response positive. Discussions with leading chip suppliers; Intersil and ADI

**Data Converters**
- Micro-converter value proposition established with ADI. NCL performance benefits enable 4x increase in product price.

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**NCL08 Product Overview**

**Baseline NCL08GP32:**
- Star8 core with BDC
- 32k x 8 FLASH memory
- 4k x 8 SRAM memory
- 16450 UART
- SPI
- KBI
- Dual Timer/Counter with PWM
- GPIO
- Clock Generator (for external circuits)
- 44 pin QFP

**Performance Goals:**
- 30% less power
- 6 dB less noise/EMI

**Actual Performance:**
- 40% less power
- 11dB less noise

**Future Enhancements:**
- We believe library improvements have the potential to further reduce power by another 10%

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(Timeless Solutions™)

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Development Issues
Designed to be an instruction set clone with Star08 advanced microcontroller architecture in TSMC’s 0.25µm technology (with support from Motorola).
NCL cell libraries developed in parallel with processor and compatible with Artisan’s 0.25µ library (including I/O pads)
Architectural improvements include enhanced bus structure, comparable instruction set unit…
Completed silicon in August 2000

Design Goals/Requirements
25MHz equivalent clock rate
30% less power than the STAR08
-6dB noise improvement over the STAR08
Keep core area small enough so minimum chip area is pad limited
### NCL08/Star08 PowerMill Results

<table>
<thead>
<tr>
<th>Power Supply Voltage</th>
<th>Temperature</th>
<th>Process</th>
<th>NCL Power Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.75</td>
<td>-40°C</td>
<td>FF</td>
<td>40.7%</td>
</tr>
<tr>
<td>2.75</td>
<td>75.0°C</td>
<td>TT</td>
<td>38.8%</td>
</tr>
<tr>
<td>2.50</td>
<td>25.0°C</td>
<td>TT</td>
<td>38.9%</td>
</tr>
<tr>
<td>2.25</td>
<td>-40°C</td>
<td>FF</td>
<td>39.9%</td>
</tr>
<tr>
<td>2.25</td>
<td>125.0</td>
<td>SS</td>
<td>37.8%</td>
</tr>
</tbody>
</table>

#### Operating Conditions
- NCL08: Voltage 2.50, Temp 25.0°C, Process TT
- STAR08: Voltage 2.75, Temp -40°C, Process FF

### NCL Design Methodology

- Design methodology based on commercially available tools
- NCL Libraries
- NCL SHELL for Orphan checking, Performance analysis, SCAN

- With $V_{dd} = 2.5V$, the NCL08 had a measured equivalent clock rate of 32.5MHz
- The NCL08 operated correctly across the voltage range with $0.9V < V_{dd} < 3.4V$ (2.5V is nominal)
- The NCL08 operated correctly across the temperature range -20°C to 80°C
Verification & Performance Modeling

Verification

- SPICE Simulations
- Verification Suites and Benchmarks

Power Modeling/Analysis

- PowerMill

Timing/Throughput

- Static timing analyzer
- Benchmark simulations
- Delay-Insensitive by design

Unique aspects

- Lack of clock tree

Test

Orphan Checking

- Pass ensures all gate switching (NULL to DATA) is observable at a primary output.

Toggle Tool for Test Vector Coverage

- In an orphan free design, a gate toggle from NULL to DATA will be observable (see above).
- The gate models monitor for minimum vector set for full coverage of the gate.

BIST

- Has been implemented for the RAM on the NCL08

SCAN

- We have a functional SCAN cell
- We are developing the software for automatic SCAN insertion

ATPG

- We can easily use commercial tools such as Synopsys’ TetraMax™
This is a product roadmap for NCL (NCL Product Roadmap) from 2002 to 2003. The roadmap is divided into two main sections: Chips and Tools.

**Chips**
- **NCL08GP32**
- **NCL08GP32 Sales**
- **3rd Party Support**
- **NCL8051 Dev**
- **NCL8051 Sales**
- **3rd Party Support**
- **High Perf DSP Dev**
- **High Perf DSP Prod**
- **High Perf DSP Sales**
- **Custom NCL08**
- **Custom NCL8051 Sales**

**Tools**
- **NCLXP Dev**
- **NCLXP Sales**

The roadmap shows timelines for the development and sales of these products, with some items marked with a downward triangle indicating a decrease or end in that timeframe.