The Application of NULL Convention Logic to
Microcontroller/Microconverter Products

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Theseus logic has designed and fabricated a reusable NULL Convention logic (NCL) 8-bit core. This core is being used to generate a family of microcontroller/microconverter products that will include both standard and custom application specific chips. This core is an instruction set accurate NCL implementation of the Motorola Star 08 CPU and is backward compatible with their HC05 and HC08 instruction sets. The core forms the nucleus of the NCL08GP32, a general-purpose microcontroller which is the first product being introduced by Theseus under a strategic alliance with Motorola. The motivation for the use of NCL is a significant reduction in power and noise/EMI compared with the equivalent clocked core. The performance of the NCL chip will be presented, and the design details and product strategy will be discussed.

The nucleus of the NCL08GP32 is the 8-bit processor core. The NCL08 CPU, memory mapping controller (MMC), interrupt unit and background debug controller (BDC) constitute the core hierarchy. Support circuitry around the core includes a 32Kx8 FLASH, 4Kx8 RAM and multi-point bus controller. System and peripheral components are accessed through a Bus Exchanger (BEX) that isolates the processor local bus from the peripherals. In actuality, it functions as a point-to-point register select bus, broadcast write data bus and shared read data bus. This bus architecture takes advantage of NCL signaling properties to reduce loading and signal switching. The peripherals for this chip consist of an 8-bit keyboard interrupt unit, two dual channel timers, a 16450 UART, a Serial Peripheral Interface (SPI), a watchdog timer and 25 general purpose IO’s (GPIO).

The NCL08GP32 contains components that communicate with generally synchronous external environment; thus an external crystal oscillator is used to drive the synchronous components.

NCL08GP32 chips and demonstration boards are currently being shipped to potential customers. A second pass design is underway to improve the FLASH memory performance and correct a serial communication interface design error.