TAST

TIMA Asynchronous Synthesis Tools

Anh Vu Dinh Duc, Jean-Baptiste Rigaud, Amine Rezzag, Antoine Siriani, Joao Fragoso, Laurent Fesquet, Marc Renaudin

Plan

- Introduction
- Design Flow
- Results
- What’s Next?
- Conclusion
Plan

- Introduction
  - Presentation of the Group
  - Presentation of the Project
- Design Flow
- Results
- What’s Next?
- Conclusion

Introduction

- Presentation of the Group
  - Lab: TIMA, Grenoble, France
  - CiS Group: Concurrent Integrated Systems
  - Contact: Marc.Renaudin@imag.fr
  - Link: http://tima.imag.fr/cis
Introduction

• Presentation of the Project
  – Competition
    ➢ Time to Market
    ➢ Time to Quality

  – Crisis
    ➢ NRE Cost Reduction
    ➢ Manufacturing Cost Reduction

• Technology
  VDSM
  • High Complexity
  • Low Voltage
  • High Defect Density

• Applications
  SoCs for Smart Devices
  • Low Power
  • Low EMI
  • High Speed
  • High Reliability
Introduction

• Presentation of the Project
  – Main Features
    • High Level of Abstraction
      – CHP
      – Petri Net
    • High Level of Automation
      – Multi-target Compiler
        » Simulation
        » Synthesis
      – Interface with Standard Tools
      – Ease of Use
  • Co-Design Platform
    – Hierarchy
    – Micropipeline, QDI, Synchronous and, Behavioral Modules
    – Design Reuse

Plan

• Introduction
• Design Flow
  – Front End Compiler
    • CHP
    • Petri Net
  – Simulation Model Generator
    • VHDL Behavioral Model
  – Synthesizer
    • DTL
    • Micropipeline
    • QDI
• Results
• What’s Next?
• Conclusion
CHP Code

TAST Compiler

TAST: TIMA ASYNCHRONOUS SYNTHESIS TOOLS

Design Flow

- CHP: Communicating Processes
  - Asynchronous Point to Point Communications
  - Parallelism
  - Guarded Commands
  - Non Determinism
  - Traceability

Specific TAST Features
- Arbitrary Precision Arithmetic
- Data Encoding (1 out of n)
- Protocol (BD/DI)
- Hierarchy
- Configuration Mechanism
TAST: TIMA ASYNCHRONOUS SYNTHESIS TOOLS

Design Flow

- Petri Net
  - Place/Transition Petri Net
  - DFG-CFG
  - Timed
  - Hierarchical
Design Flow

- Simulation
  - VHDL Behavioral Model
    - CHP Component = Entity/Architecture
    - CHP Process = VHDL Process
    - Each Place of the Petri Net gives a state signal
    - Each Primitive in the Petri Net gives a VHDL sequential bloc in the VHDL Process
    - Trace is obtained through VHDL assertions
    - Non Determinism is managed through a VHDL random generator and a SEED
Design Flow

• Synthesis
  – DTL: Specifications for a Synthesizable CHP
  • Shared variables are forbidden
    – a := b + c, a := d + e; FORBIDDEN
  • Variables must be assigned before they are read
    – x := x + 1; FORBIDDEN
  • Values sent to output channels must only depend on values received from input channels
    – Concept of Combinatorial Process
  • Output channels can be initialized once at the beginning of the process
    – [S!F.F.F[16][3]; ...] ALLOWED
  • Sequential access to variables must exhibit true dependency
    – a := b + c; d := e; FORBIDDEN
    – S!x; $S!x$ FORBIDDEN
Design Flow

- Synthesis
  - DTL: Extraction of a Memorization Element

Combinatorial Process

Register

Inputs
  - Read

Outputs
  - Write
Design Flow

• Synthesis
  – QDI Synthesis
    • Equation Dependency Generation
    • Protocol Selection
    • Gate Netlist Generation
    • Optimization
    • Mapping onto VHDL Standard Cell Libraries
Design Flow

- Synthesis
  - Micropipeline Synthesis
    - Target Architecture:
      - Data path is extracted from DFG Part
        - It is synthesized with Standard Tools
      - Petri Net (CFG) is synthesized in the same way than QDI except that Ports are turned to Single-Rail
      - Delays are added to compensate Guard Computation Delays and Enable to Output Delays

TAST: TIMA ASYNCHRONOUS SYNTHESIS TOOLS

- Low Power
- Low Voltage
- Low Noise

Simulation Model Generator
  - Behavioral Asynchronous VHDL Model
  - VHDL Custom Libraries for Simulation

TAST Model Generator
  - Reports
  - VHDL Simulator

Standard Design Flow
  - Back-end Tools

GALS, GALA SoCs
- Secure Smart-Cards
- Smart Devices

Current profiles (Mica processors)
Plan

• Introduction
• Design Flow
• Results
  – CHP Code Example
  – VHDL Behavioral Model
  – Micropipeline Synthesis
  – QDI Synthesis
• What’s Next?
• Conclusion

Results

• CHP Code Example:
  – A Counter 0 to 6
    • Non DTL Compliant Code
      
      ```vhdl
      COMPONENT counter
      PORT (GO: IN DI PASSIVE SR; S: OUT DI ACTIVE BIT[2..0])
      BEGIN
      PROCESS main
      PORT (
        GO: IN DI PASSIVE SR; S: OUT DI ACTIVE BIT[2..0]
      )
      VARIABLE x : bit[2..0]:
      [x:=0; x<7 => S=x; x:=x+1
      @ x=7 => x:=0; GO?])
      END counter;
      ```
Results

• CHP Code Example:
  – A Counter 0 to 6
  • DTL Compliant Code

```vhdl
COMPONENT counter
PORT (GO: IN DI PASSIVE SR;
      S: OUT DI ACTIVE BIT[2:0])
CHANNEL CS, NS: DI BIT[2:0];
BEGIN
  PROCESS MAIN
  PORT (GO: IN DI PASSIVE SR;
       CS: IN DI ACTIVE BIT[2:0];
       NS: OUT DI ACTIVE BIT[2:0];
       S: OUT DI ACTIVE BIT[2:0])
  VARIABLE cs_v: BIT[2..0];
  [cs_v] = "1.1.1" => NS?cs_v,
  S!cs_v;
  [cs_v] = "0.0.0" => GO?cs_v,
  NS!cs_v;
  END counter;
```
Results

• QDI Circuit: Process Main

Results

• QDI Circuit: Process Increase
Results

• Micropipeline Circuit: Process Main

• Micropipeline Circuit: Process Increase
Plan

• Introduction
• Design Flow
• Results
• What’s Next?
• Conclusion

What’s Next?

• C Simulation Models
• VHDL Entry
• Logic Optimization
  – Exploration of Various Protocols
  – On-the-fly Complex Cell Generation
  – Exploration of Various Data Encoding
• Prototyping QDI Circuits with FPGAs
Plan

- Introduction
- Design Flow
- Results
- What’s Next?
- Conclusion

Conclusion

- What to keep in mind?
  - Weaknesses
    - Optimization
    - Maturity
  - Strengths
    - High Level of Abstraction
    - High Level of Automation
    - 1 out of N Arithmetic
    - Co-Design Framework
    - Address VDSM SoCs
- Perspective
  Offer a set of CAD Tools to Design Efficient Asynchronous VLSI Circuits and allow Designers to make the Best Trade-offs for their Applications.
Thank You