**Motivations**
Asynchronous digital system and its circuit design technologies offer a smart alternative to a number of limitations faced by synchronous methodologies, mainly in the field of very deep submicron SoC (System on a Chip) design. Nonetheless, the semiconductor industry needs efficient CAD/EDA tools and IPs to take benefit of these promising technologies.

**Inputs**
We have developed a proprietary high level description language derived from CHP (Communicating Hardware Processes) with specific features to cope with communication protocols, data encoding, arbitrary precision arithmetic, non-deterministic data flow, hierarchy, project management and, traceability. All these features make our modified CHP a very practical system description language to develop with. Moreover, it makes scalability and modularity easy to manage. Of course, this is of a paramount importance in the field of very deep submicron SoC design.

**Outputs**
TAST engine is able to address three kinds of targets from a modified CHP input program:
- Behavioral VHDL simulation models,
- Micropipeline style VHDL gate level asynchronous circuits,
- QDI (Quasi Delay Insensitive) style VHDL gate level circuits.

**Presentation**
The presentation is focused on the asynchronous digital circuits design flow using TAST CAD tools. It will demonstrate various up-to-date features of the tool suite, mainly simulation model generation, QDI and micropipeline circuit synthesis. Future developments will be considered as well.

**Abstract**
TAST is the acronym for TIMA Asynchronous Synthesis Tools. It mainly consists of a compiler/synthesizer with the capability of targeting several outputs from a high level CSP-like description language. The flow is organized around Petri Nets (PNs) associated to Data Flow Graphs (DFGs). Such a model has been used for years to describe synchronous circuits and systems. However, it finds a particularly adequate application in the field of asynchronous digital circuits and systems design.

Asynchronous digital circuit synthesis is based upon DTL (Data Transfer Logic) specification. It provides a set of rules to guarantee that PN-DFG graphs are synthesizable into asynchronous digital circuits.

**Future Plans**
We are currently finalizing an early version of the tool. It integrates every mentioned feature with a high level of quality. Notably is at stake the performance of the synthesized circuits in terms of area, speed, power and EMI (Electro Magnetic Interference) noise.

Some cutting-edge features will appear soon:
- A VHDL synthesizable RTL simulation model target to address prototyping (ASIC, FPGAs …).
- A C self executable simulation model target to address high speed simulation.