Design Flow and CAD tools for asynchronous design of sequential library cells

Cédric Cuche (1), Christian Piguet (1, 2), Vojin G. Oklobdzija (3)

1. LAP-EPFL, Lausanne, Switzerland
2. CSEM, Neuchâtel, Switzerland
3. University of California Davis, CA 95616 U.S.A.

The design of “small” Speed-Independent sequential library cells, such as Flip-Flops, can be performed using STG-based (Signal Transition Graph) methodologies. Starting from a STG that is adapted to produce only negative logical equations, this method has been used for manual design of many basic cells. However, a more automatic approach could be beneficial. CAD tools and a design flow on PC Windows implementing this methodology will be presented, including existing tools such as Petrify, as well as new CAD tools that are capable of verifying if the produced cells are SI or not. The logical equations of the considered cell or the logical equations of the N-ch and P-ch networks are analysed to produce the flow table of the cell as well as an analysis of the possible critical races. In case of critical races, the considered cell is not SI. The design flow is not completely automatic, as logical equations produced by Petrify from a “negative” STG are not always in suitable forms.

The presented design flow has been used for the design of several different basic cells, including D-Flip-Flops and other various “small” asynchronous Finite State Machines. The presented CAD tools are also interesting in case of critical races, i.e. in case of not SI circuits. For some circuits, the transistor schematic is simpler and faster than the SI circuit implementing the same behaviour. The complete description of the race between two logical gates switching at the same time is available, for both cases in which the first or the other logic gate is faster than the other one. It is therefore possible to check the conditions on the gate delays for a correct behaviour.

A special non SI D-Flip-Flop circuit, i.e. containing critical races, will be presented as an example. This circuit has been patented, and has been analyzed and compared with nearly all the other D-Flip-Flop types in very deep submicron technology. The results show that it is one the best D-Flip-Flop structure if only pure and robust static logic is considered.