"Designing an asynchronous Microcontroller using Pipefitter"

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In the last few years, number of efforts have been made to bring asynchronous design flows on a par with its synchronous counterpart, as the latest stage of a long effort to push this promising and theoretically clean design style into mainstream use.

The Tangram group at Philips Research has long promoted the use of a flow based on a proprietary, Communicating Sequential Processes-based language, and relying on a proprietary tool set. While this is excellent in a research environment within Philips, the proprietary nature of the tools, and the requirement to train designers to the art of "VLSI programming" makes practical widespread adoption of this methodology in the short and medium term problematic. However, our work has been heavily influenced by the work of the Tangram group, as well as by that of Martin's group at CalTech, and of the Balsa group at Manchester University.

We believe, though, that practical asynchronous design requires standard languages and (as much as possible) standard tools.

Our approach, embodied in the Pipefitter tool, provides exactly an asynchronous ASIC-style design flow, based on a standard language (Verilog) and using a specially developed tool only to: - perform the asynchronous equivalent of RTL (and optionally high-level) synthesis, - manage the overall flow, by generating the appropriate scripts and calling the appropriate synchronous Electronic Design Automation tools.

It gives up some optimality, both in the choice of specification language, and in the implementation of the controller, to gain in terms of widespread applicability and ease of use. It is thus suited for fast-turnaround design cycles of low-performance circuits with low or medium production volumes, but, for example, stringent electro-magnetic emission or low-power requirements. While this is by no means a majority of the designs around, it is a significant (growing) fraction of ASICs.

This presentation discusses how Pipefitter, a tool chain that implements a fully automated synthesis flow for asynchronous circuits, can be used to design a simple asynchronous microcontroller. The use of RTL-like Verilog HDL as the input format makes the first steps of the design flow (i.e. specification and simulation) very easy for the designer.

Pipefitter directly synthesizes the Control Unit as a hazard-free standard cell netlist, uses a genetic algorithm to perform binding and multiplexer optimization for the Data Path, allows the user to manually specify the binding, and can automatically pipeline a sequential specification. It also produces a synthesizable Verilog specification for the Data Path, as well as a set of scripts driving both its synthesis and timing analysis by state-of-the-art commercial synchronous RTL and logic synthesis tools. The automated insertion of matched delays completes the logic design, and hands off the netlist to the standard cell-based layout tools.

The example presented shows how Pipefitter can be effectively used for the design of asynchronous Application Specific Integrated Circuits.