AsynchronSparc

A asynchron redesign of a chip under the OpenSource-paradigma.

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In the last years through Sun Microsystems with the microSPARC IIep and ESA with the Leon two SPARC V8 Processor Designs became available for everybody. So its the first time that the layout of a mainstream Instruction Set is available for the public. But will this publication also help the asynchron redesign of a chip. And is it possible that a asynchron version of a mainstream chip will help also other asynchron designs to succeed on the market place. Or to make decisions about what tools should be used in future to design or redesign circuitry. Because the big advantage of the OpenSource-paradigma and a OpenSource project is the theoretical unlimited manpower and not to be fixed on a design-team. Are the tools and the redesign different under this new paradigm? I started a OpenSource project with the goal to redesign a V8 SPARC-layout into a self-timed circuitry. The bounded-delay model with micropipelines will be used but I also will do a evaluation if a dual-rail encoding implementation makes sense under the new paradigm. And if a V8 SPARC-layout is redesignable in that way. Further I will investigate if VHDL is useable as description-language for a asynchron redesign of a chip.