A structural encoding technique
for the synthesis of asynchronous circuits

Josep Carmona    Jordi Cortadella    Enric Pastor

Encoding the state space is one of the main problems in the synthesis of asynchronous circuits. Most existing techniques work at the state-level, thus suffering from the well-known state explosion problem.

In this talk we will present an encoding technique performed at the Petri Net level in such a way that a circuit implementation is always guaranteed. The encoding technique is based on the insertion of new internal signals that mimic the token flow of the original STG. Depending on the original STG, the signal insertion can be done preserving the I/O interface.

Moreover, a set of transformations is presented for the subclass of Free-Choice Petri nets that enables the exploration of different solutions. All transformations preserve the property of free-choiceness, liveness and safeness, thus enabling the use of structural methods for the synthesis of asynchronous circuits. The transformations are concurrency reduction, increase of concurrency, elimination of signal, elimination of silent transitions and elimination of redundant places. The application of these transformations can be guided either by the designer or heuristically.

Experimental results performed automatically show that this new synthesis methodology is comparable with those that work at the state level. In a near future, a complete automation of the application of the transformations (using some optimization techniques like Genetic algorithms or Tabu Search) will enable an efficient exploration of the solution space.

The main purpose of this work is to provide logic synthesis tools that can handle large control specifications generated from hardware description languages.