1-of-4 Globally Asynchronous Interconnect

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- Problems with wires
- Latch controller performance
- DI alternatives to bundled data
- 1-of-4 Transition signalling
- 1-of-4 Level signalling
- Packet comms issues
- Example application: MARBLE replacement

Problems with wires

- Wires have resistance, $R$
- Parallel wires are coupled
- Coupling mostly due to $C$
- Signal propagation speed depends upon $RC$
- Data-dependent variation in propagation speed with parallel interconnections
Area Implications

- The delay and its variation make it even more difficult to ensure bundling constraints are met - need 100% margin in the worst case
Latch controller performance

<table>
<thead>
<tr>
<th></th>
<th>Normally-closed (ns)</th>
<th>Normally-open (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>forward latency</td>
<td>0.9</td>
<td>0.6</td>
</tr>
<tr>
<td>input latching time</td>
<td>1.7</td>
<td>0.9</td>
</tr>
<tr>
<td>total input cycle time</td>
<td>2.2</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Delay Insensitive alternatives to bundled data

- Remove the need for margin
- Incur an area/power penalty

<table>
<thead>
<tr>
<th>Bits/wire</th>
<th>Transitions/bit (NRTZ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>single-rail</td>
<td>1</td>
</tr>
<tr>
<td>dual-rail</td>
<td>1/2</td>
</tr>
<tr>
<td>1-of-4</td>
<td>2/4</td>
</tr>
<tr>
<td>3-of-6</td>
<td>4/6</td>
</tr>
<tr>
<td>2-of-7</td>
<td>4/7</td>
</tr>
<tr>
<td>3-of-8</td>
<td>5/8</td>
</tr>
<tr>
<td>2-of-9</td>
<td>5/9</td>
</tr>
</tbody>
</table>

- But, completion detection is required!
Wire layout for 1-of-4 signalling protocol

- Two data-wires per bit
- A transition conveys one bit
- Simple pipeline latch
Transition Signalling - 1-of-4

- Four data wires per group
- A transition conveys one of four symbols (each 2 bits): 00, 01, 10 or 11
- Simple pipeline latch
- BUT 4-input XOR is large/slow

Improved 1-of-4 Transition Signalling Latch
1-of-4 Level Signalling

- Simpler than transition signalling
- RTZ takes time, but no slow XOR gates

- ~500 MHz operation, i.e. 1Gb/s with short wires between stages

Performance comparison

- Faster than bundled data for narrow datapaths
- Wider datapaths require completion detection across groups:
  - 8 bit datapath => 4 input C-element => 700 Mb/s/group
  - 32 bit datapath => 16 input C-element => 550Mb/s/group
- About the same throughput for wide datapaths (2x wire cost)
- If completion detection is only performed at each end, then we can multiplex the use of the link:
  - same overall end-end throughput as above
  - BUT using half as many groups (same wire cost as bundled data)

no good reason to use bundled data for global interconnect
Select and Merge Components

Packet Format

- How do we detect the start/end of a packet?
  - special symbols
  - fixed length packets
Packet Arbitration

Interconnect Topology

- Header extraction, steering, merging and arbitration are all we need to build packet switches allowing the choice of using a
  - Ring network
  - Switched hub / star network
  - Multiplex - demultiplex ‘bus’ type arrangement
Example: MARBLE Replacement

- high performance requirement
- chain multiple 1-of-4 links in parallel
- 4 parallel links -> 4Gb/s
- must ensure that:
  - all select units switch packets to the same output
  - all merge units accept packets from the same input
- Use three such links for address, write-data and read-data
Summary

- Bundled data unsuitable for global interconnect
- Similar performance at similar cost can be achieved with 1-of-4
- 1-of-4 level based switched networks are a feasible replacement for bundled-data system buses